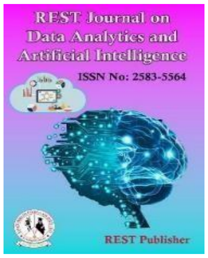
REST Journal on Data Analytics and Artificial Intelligence
Vol: 4(2), June 2025
REST Publisher; ISSN: 2583-5564
Website: http://restpublisher.com/journals/jdaai/
DOI: https://doi.org/10.46632/jdaai/4/2/10



Improving Fault-Tolerance in Nano-Computing Circuits Through Design Optimization Using the Electric Method

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***Abstract:** Nano-Computing. Nano-computing is an emerging field at the intersection of nanotechnology and computing, aimed at developing ultra-small and highly efficient computing systems. By leveraging nanomaterials and nanoscale devices, nano-computing promises to revolutionize traditional computing paradigms, offering unprecedented computing power and compactness. The use of nanoscale components enables faster information processing and lower energy consumption, paving the way for advancements in areas like artificial intelligence, data storage, and medical applications. As researchers delve into the potential of nanocomputing, it opens up exciting possibilities for the future of computing technology. Nano-computing research holds immense significance as it explores the potential of nanoscale materials and devices to revolutionize computing technology. The development of ultra-small and highly efficient computing systems can lead to groundbreaking advancements in various fields, including medicine, electronics, and data processing. Nano-computing offers the promise of unprecedented computing power and energy efficiency, enabling faster information processing and new computing paradigms. The exploration of nanocomputing's capabilities could lead to transformative breakthroughs in artificial intelligence, quantum computing, and data storage, ultimately shaping the future of computing and its impact on society. Methodology: The ELECTRIC method, short for Elimination and Choice Expressing Reality, is a multi-criteria decision-making technique used to assess various alternatives based on multiple criteria. The method involves two stages. First, it eliminates unrealistic options that do not meet the necessary criteria. Next, it helps decision-makers express their preferences by ranking the remaining alternatives. By assigning weightage to each criterion and considering the expressed preferences, the ELECTRIC method quantitatively evaluates the alternatives and identifies the best choice. This method is particularly useful when dealing with complex decision-making scenarios where multiple criteria need to be considered to make a well-informed and objective choice. Alternative: Processing Speed (GHz), Energy Efficiency, Memory Capacity (gigabytes), Scalability, Error Rate, Parallelism. Evaluation preference: Quantum Dot Nanocomputing, DNA Nanocomputing, Carbon Nanotube Nanocomputing, Molecular Nanocomputing. Results: From the result it is seen that Incident Response is got the first rank where as is the Scalability is having the lowest rank.*

Keywords: *Quantum Dot Nanocomputing, Carbon Nanotube Nanocomputing, Molecular Nanocomputing, ELECTRIC*

1. INTRODUCTION

Nano-Computing model based on the Moore engine, which simulates neuro-spike communication within the human body. It involves sensing input spikes and generating signals by the actuator to complete the entire life cycle of neuropile communication. This approach offers promising potential for understanding and controlling vital processes at the nanoscale level. Drawing insights from the biology of intraneuronal communication and Moore's mechanical principles, the research aims to identify the underlying principles governing axonal spike communication between neurons. The ultimate goal is to design a Nano-Computing model that can address various diseases arising from faulty intracellular and inter-tissue communication in the human body, enabling precise diagnosis and targeted drug delivery. [1] nanoscale devices are anticipated to become more delicate and susceptible to external influences compared to current CMOS-based devices. Researchers predict that testing these nanoscale devices will no longer be feasible, and if any faults are detected, the devices will be discarded instead of being repaired. As each testing round progresses, the difficulty in identifying and dealing with defects is expected to increase, especially with regards to soft defects. In response to this challenge, new fault-tolerance structures are being developed to create robust systems that can withstand manufacturing defects and transient faults. One such technique is the History of Exact Calculation Schedule (HICC), which is an operation used for fault-tolerant nanocomputing reconstruction. [2] The process of intraneuronal communication is akin to nano networking, and it plays a crucial role in the development, diagnosis, and solutions of various diseases. A novel exploratory Nano-Computing model is proposed in this study to emulate the intricate communication patterns between nerve cells. The model is based on the Moore machine, modified and adapted for nanoscale neuro-spike communication within the body. Nanonetworks serve as a fascinating example of multimodal communication within the human body, integrating nervous, cardiovascular, and endocrine networks, among others. In this context, the internal nerve communication within the body performs vital functions, acting as a Nano-Computing that inspires the creation of artificial systems capable of controlling specific tasks when activated.[3] In the realm of nanoscale computing, achieving a precise manufacturing process for devices remains uncertain, but the future technology holds promise and clarity. There is a likelihood of increased defect rates in nodes, making it imperative to develop new architecture and design methodologies that can effectively handle a substantial number of defects. One crucial aspect is constructing defect diagrams within future design flows, necessitating practical research and implementation. In this context, Bloom filters serve as data structures to represent defective maps. Our investigation focuses on the accuracy and space efficiency of Bloom filters, which facilitate seamless exchanges between nano systems, ultimately contributing to streamlined nano system design. [4] We propose a novel approach to embed defect information within a given nano system, addressing the concerns of manufacturers in nano-sized memory designs. By adopting this concept, we establish a voting strategy that is not reliant on existing approaches or device redundancy, leading to a highly effective utilization of resources. The prototype of nanoscale devices is constructed using chemical assembly, diverging from the traditional top-down lithography seen in VLSI manufacturing over the past decades. This progress brings hope for the future, where computer peripherals can work with unprecedented density (around 10^10 devices/cm^2) in the THz frequency domain.[5] There are fundamental differences between traditional methods and proposed nanoscale methods in manufacturing. Nanoscale techniques offer complexity and structures that cannot be replicated in today's ASIC designs, instead focusing on regular, periodic, and programmable structures resembling natural nanoscale structures. Nanoscale devices are predicted to have high defect rates, which can be categorized into two types: (i) inherent permanence due to physical uncertainties in the production process and (ii) transient faults caused by noise tolerance or reduced voltage and current injection. Self-assembly of nanometer devices can lead to defect rates as high as 10%, much worse compared to the billion defects found in current CMOS technology.[6] To address the issue of defects in nanocomputing devices, various fault-tolerance design methods and architectures are proposed. These methods fall into two categories: redundancy-based approaches, like R-Fold Volume Redundancy (RMR), which can handle both permanent defects and transient faults; and reconfigurable techniques that offer post-production design to effectively handle defects. Among the reconfigurable approaches, Bloom filters prove to be an attractive data structure to deal with defects. They effectively handle production defect ratios ranging from 0.01 to 0.1. However, they may not be stable enough to handle errors effectively, which is a drawback of this approach.[7] In this work, the focus is on novel defect tolerance using Bloom filters in a scaled memory architecture for nanoscale devices. This approach eliminates the need for traditional majority polling methods, making it more efficient in handling permanent impairment tolerance. Handling transient errors is within the scope of future work. To the best of our knowledge, this is the first attempt to use Bloom filters for defect-tolerant computing in nanoscale devices.[8] Nano computing refers to the field of computing that operates at the nanoscale, utilizing nanomaterials and nanodevices to perform computational tasks. The main goal of nano computing is to create highly efficient and powerful computing systems that are significantly smaller and faster than current technologies. These nanoscale devices have unique properties that can lead to advancements in various applications, including medicine, electronics, and data processing.[9] Nanoscale manufacturing techniques, such as chemical assembly, enable the construction of nanoscale devices. These methods differ from traditional top-down lithography used in VLSI manufacturing and offer regular, periodic, and programmable structures, resembling natural nanoscale structures. One of the key challenges in nano computing is handling defects and errors that arise due to the intricacies of nanoscale manufacturing. High defect rates, both permanent and transient, pose significant hurdles in developing reliable and fault-tolerant nanoscale devices.[10] Researchers have proposed various fault-tolerance design methods and architectures to address these defects. Among them, reconfigurable techniques using data structures like Bloom filters have shown promise in effectively handling defects and improving fault tolerance. Despite the challenges, nano computing holds great promise for the future. It offers the potential for unparalleled computing power, density, and speed in the THz frequency domain. With ongoing research and advancements, nano computing could revolutionize various industries and pave the way for next-generation computing systems with extraordinary capabilities. [11] The foundation of dispersion costs in nanocomputing is established on designing lower limits specifically for nanocomputing examples. It can offer valuable insights into various aspects, such as the authenticity and finality of CMOS nanocomputing projects. However, there are limitations to consider. The basis of Landauer's theory is fundamentally rooted in considerations for visualizing and properly utilizing isolated memory components or gates, which can be more complex than anticipated. For more intricate circuits, useful estimates of dispersion costs can be directly obtained from circuit simulations. Nevertheless, simulations may not reveal the basic lower bounds as the results are unique and depend on detailed geometries, device choices, sample selections, and the numerical values used to parameterize these models.[12] The underlying basis for understanding the unavoidable dispersion in nanocomputing lies in determining the limits through actual examples and calculating costs. This involves applying basic physical laws directly to the nanocomputing paradigm, which defines the fundamental computational strategy for representing and handling information in both space and time. Physicists often utilize fabric representations to simplify calculations and make them useful. To obtain achievable and robust limits in this nature, it is essential to consider the perspective of trivial nanocomputing with clock views, multigate digital circuits, and generally irreversible logic functions. These circuits functionally process input data streams, which lead to changes in source and output data destined for external destinations. [13] Carbon nanostructures have led to the creation of numerous nanodevices, particularly carbon nanotubes, which have garnered significant attention due to their mechanical, electronic, and energy properties. Of particular interest is the internal storage capacity accessible through the open ends of carbon nanotubes, which can be filled by other molecular structures. [14] The current study holds significance in analyzing and deriving expressions for energy calculations, providing explicit formulas in the appendices for spheroidal fullerenes and nanotubes. Detailed treatment of acute gradients and offset configurations can be found in Appendix J, which involves evaluating coordinates and can be more complicated than initially perceived, requiring careful consideration of any approximations or numerical integration methods.[15] The most intriguing result of this research is the identification of two local minima for some critical radii, where the exit becomes equally dominant. Specifically, the critical radii are 8 Å for C_{70} molecules and 8.3 Å for C_{80} molecules. These structures offer a promising situation for nano-computing, as they may provide exploitable configurations for memory devices.[16].

2. MATERIALS & METHODS

Alternative:

Processing Speed (GHz): This metric measures the speed at which a nanocomputing can perform calculations or process data. Higher processing speed indicates that the nanocomputing can execute tasks more quickly.

Energy Efficiency: Energy efficiency measures how effectively a nanocomputing utilizes energy to perform computations. A higher energy efficiency means that the nanocomputing consumes less power to accomplish tasks.

Memory Capacity (gigabytes): Memory capacity refers to the amount of data that a nanocomputing can store and access. Higher memory capacity allows the nanocomputing to handle larger datasets and perform more complex computations.

Scalability: Scalability evaluates how well the nanocomputing can adapt and handle increasing computational demands. A highly scalable nanocomputing can accommodate more resources and tasks without compromising performance.

Error Rate: Error rate indicates the accuracy and reliability of the nanocomputing computations. Lower error rate means the nanocomputing produces more accurate results.

Parallelism: Parallelism measures the ability of the nanocomputing to perform multiple tasks or computations simultaneously. Higher parallelism enables faster and more efficient processing of tasks.

Evaluation preference:

Quantum Dot Nanocomputing:

Quantum dot nanocomputing involves the use of quantum dots as the building blocks for nano computer devices. Quantum dots are semiconductor nanocrystals that exhibit unique quantum mechanical properties, allowing them to manipulate and store information at the quantum level. Quantum dot nanocomputing shows promise in achieving high processing speeds and energy efficiency due to quantum effects.

DNA Nanocomputing:

DNA nanocomputing leverages the self-assembly properties of DNA molecules to perform computations and store data. DNA molecules can be programmed to act as logic gates and perform calculations through chemical reactions. DNA nanocomputing has potential for high memory capacity and data storage, but it currently faces challenges in terms of processing speed and error rates.

Carbon Nanotube Nanocomputing:

Carbon nanotube nanocomputing uses carbon nanotubes as the fundamental building blocks for nano computer components. Carbon nanotubes possess excellent electrical and mechanical properties, making them suitable for nanoscale computing. Carbon nanotube nanocomputing shows promise in terms of scalability and energy efficiency, enabling high-performance computing.

Molecular Nanocomputing:

Molecular nanocomputing involves utilizing individual molecules as computational elements. It leverages the unique properties and interactions of molecules to perform calculations and store information. Molecular nanocomputing has the potential for high parallelism and can operate at the atomic scale, enabling novel computing paradigms.

3. ELECTRIC METHOD

The ELECTRIC method, which stands for Elimination and Choice Expressing Reality, is a powerful and effective multi-criteria decision-making technique. It is designed to assist decision-makers in evaluating various alternatives based on multiple criteria and selecting the best option among them. The method involves two primary stages: elimination and choice.[17] In the elimination stage, decision-makers systematically eliminate alternatives that do not satisfy essential criteria or are considered infeasible or unrealistic. This step helps to focus on the viable options and streamlines the decision-making process. The elimination stage is essential in narrowing down the set of alternatives, ensuring that only relevant and feasible options remain for further consideration. In the choice stage, decision-makers express their preferences for the remaining alternatives by ranking them based on their desirability or suitability.[18] This step allows the decision-makers to subjectively evaluate the options and highlight their preferences, which adds a human element to the decision-making process. To apply the ELECTRIC method effectively, decision-makers must establish a set of criteria that are relevant and critical to the decision at hand. These criteria should be measurable and quantifiable to ensure an objective evaluation of the alternatives. [19] Each criterion is assigned a weightage to represent its relative importance in the decision-making process. The weightages reflect the decision-makers' priorities and help in the final evaluation. [20] After the elimination and choice stages, the ELECTRIC method calculates an ELECTRE index for each alternative, which is a numerical representation of the desirability or preference of the alternative compared to other options. The ELECTRE index is derived by considering both the preferences expressed in the choice stage and the weights assigned to the criteria. The final step of the ELECTRIC method involves ranking the alternatives based on their ELECTRE index scores. [21] The alternative with the highest ELECTRE index represents the most preferred option, while those with lower scores are ranked accordingly. The ELECTRIC method is particularly useful in complex decision-making scenarios where there are multiple criteria and uncertainties involved. [22] By systematically eliminating infeasible alternatives and incorporating subjective preferences, the ELECTRIC method helps decision-makers make informed and rational choices that align with their objectives and priorities. Its flexibility and ability to handle both qualitative and quantitative data make it a valuable tool in various fields, including engineering, finance, and environmental decision-making.[23]

STEPS INVOLVED

STEP I: Forming of Decision-Making matrix (DMM)

The under-mentioned DMM of preferences (xij) for m alternatives (rows) rated on n criteria (columns)

$$\begin{bmatrix} x_{01} & x_{02} & \cdots & x_{02} \\ x_{11} & x_{12} & \cdots & x_{1n} \\ \vdots & \vdots & \vdots & \vdots \\ \vdots & \vdots & \vdots & \vdots \\ \vdots & \vdots & \vdots & \vdots \\ x_{m1} & x_{n1} & \cdots & x_{mn} \end{bmatrix} \quad \text{I} = 0,1,\ldots,\text{m} \; ; \; \text{j} = 1,2,\ldots,\text{n}$$

STEP II: Normalize the matrix and find the weighted normalized matrix

$$r_{ij} = \frac{x_{ij}}{\sqrt{\sum_{i=1}^{m} x_{ij}^2}}, i = 1,2,\ldots,n \qquad j = 1,2,\ldots.,m$$

$$\begin{bmatrix} r_{11} & w_1 & \cdots r_{12} & w_2 & \cdots & r_{1n} & w_n \\ r_{21} & w_{n1} & \cdots r_{22} & w_2 & \cdots & r_{2n} & w_n \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ r_{m1} & w_1 & r_{m2} & w_2 & \cdots & r_{mn} & w_n \end{bmatrix}$$

STEP III: Find the concordance and discordance interval sets

Let A= {a,b,c,…} denote a finite set of alternatives in the following formulation we divide the attribute sets into two different sets of concordance interval set (Cab) and discordance interval set (Dab).

The concordance interval set is applied to describe the dominance query

$$C_{ab} = \{j | x_{aj} \geq x_{bj}\}$$

The discordance interval set (Dab)

$$D_{ab} = \{j | x_{aj} < x_{bj}\} = J - \mathrm{C_{ab}}$$

STEP IV: Calculation of the concordance interval matrix

$$C_{ab} = \sum_{j \in \mathrm{C_{ab}}} w_j$$

The concordance index indicates the preference of the assertion "A outranks B" The concordance interval matrix can be formulated as follows.

$$\begin{bmatrix} - & \mathrm{c}(1,2) & \cdots & \mathrm{c}(1,m) \\ \mathrm{c}(2,1) & - & \cdots & \mathrm{c}(2,m) \\ \vdots & \vdots & \ddots & \vdots \\ \mathrm{c}(m,1) & \mathrm{c}(m,2) & \vdots & - \end{bmatrix}$$

STEP V: Calculation of the discordance interval matrix

The discordance index of d(a,b), which can be viewed as the preference of discontent in decision of scheme a than scheme b.

$$\mathrm{d(a,b)} = \frac{\max_{j \in D_{ab}} |v_{aj} - v_{bj}|}{\max_{j \in j,m,n \in 1} |v_{mj} - v_{nj}|}$$

$$D = \begin{vmatrix} - & d(1,2) & \cdots & d(1,m) \\ d(2,1) & - & \cdots & d(2,m) \\ \cdots & \cdots & \ddots & \vdots \\ d(m,1) & d(m,2) & \cdots & - \end{vmatrix}$$

STEP VI: Determine the concordance index matrix

The concordance index matrix for satisfaction measurement problem can be written as follows

$$\bar{\mathrm{c}} = \sum_{a=1}^{m} \sum_{b}^{m} c(a,b) \,/\, m(m-1)$$

Here $\bar{\mathrm{c}}$ is the critical value, which can be determined by average dominance index, Thus, a Boolean matrix (E) is given by

$$\begin{cases} e(a,b) = 1 \;\; if \;\; c(a,b) \geq \bar{\mathrm{c}} \\ e(a,b) = 0 \;\; if \;\; c(a,b) < \bar{\mathrm{c}} \end{cases}$$

STEP VII: Determine the discordance index matrix

The preference of dissatisfaction can be measured by discordance index

$$\bar{\mathrm{d}} = \frac{\sum_{a=1}^{m} \sum_{b}^{m} d(a,b)}{m(m-1)}$$

Based on the discordance index mentioned above, the discordance index matrix (F) is given by

$$\begin{cases} f(a,b) = 1 \ \ if \ d(a,b) \leq \bar{\mathrm{d}} \\ f(a,b) = 0 \ \ if \ d(a,b) > \bar{\mathrm{d}} \end{cases}$$

STEP VIII: Calculate the net superior and inferior value

Let c_a and d_a be the net superior and net inferior value respectively. c_a sums together the number of competitive superiority for all alternatives, and the more and bigger, the better. The c_a is given by

$$c_a = \sum_{b=1}^{n} c_{(a,b)} - \sum_{b=1}^{n} c_{(b,a)}$$

On the contrary, d_a is used to determine the number of inferiority ranking the alternatives

$$d_a = \sum_{b=1}^{n} d_{(a,b)} - \sum_{b=1}^{n} d_{(b,a)}.$$

4. RESULT AND DISCUSSION

TABLE 1. Alternative:

Processing Speed (GHz)-C1

Energy Efficiency-C2

Memory Capacity (gigabytes)-C3

Scalability-C4

Error Rate-C5

Parallelism-C6

Evaluation preference:

Quantum Dot Nanocomputing-M1

DNA Nanocomputing-M2

Carbon Nanotube Nanocomputing-M3

Molecular Nanocomputing-M4

TABLE 1. Nano-Computing

	C1	C2	C3	C4	C5	C6
M1	10	0.01	32	7	2	4
M2	1	0.001	8	4	1	2
M3	5	0.005	64	9	3	5
M4	8	0.008	128	6	2	3

Table 1 provides a comparison of four nano-computing alternatives based on six evaluation parameters: processing speed, energy efficiency, memory capacity, scalability, error rate, and parallelism. Quantum Dot Nanocomputing exhibits the highest processing speed of 10 GHz, making it the fastest option among the alternatives. However, it has the lowest energy efficiency and memory capacity, with an energy efficiency of 0.01 and a memory capacity of 32 gigabytes. DNA Nanocomputing, on the other hand, has the lowest processing speed of 1 GHz but offers the highest energy efficiency and scalability among the alternatives, with energy efficiency of 0.001 and a scalability rating of 4. Carbon Nanotube Nanocomputing strikes a balance between speed, energy efficiency, and memory capacity, with processing speed, energy efficiency, and memory capacity at 5 GHz, 0.005, and 64 gigabytes, respectively. It also boasts a high parallelism rating of 5. Molecular Nanocomputing showcases a processing speed of 8 GHz, an energy efficiency of 0.008, and a memory capacity of 128 gigabytes. It is on par with Quantum Dot Nanocomputing regarding error rate and parallelism. This table highlights the trade-offs and unique characteristics of each nano-computing alternative, providing valuable insights for decision-makers to identify the most suitable option based on their specific requirements and priorities.

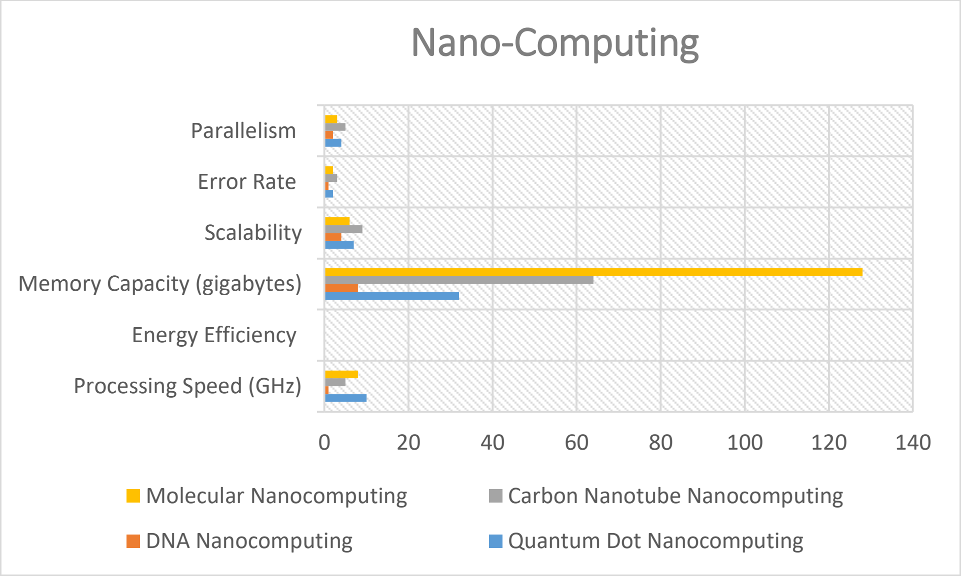

FIGURE 1. Nano-Computing

Figure 1 shows the indicates that molecular nanocomputing exhibits the highest level of parallelism, but it also has the highest error rate. On the other hand, DNA nanocomputing displays the lowest error rate, but it lacks scalability. Carbon nanotube and quantum dot nanocomputing lie in the middle with moderate performance. the graph reveals that memory capacity, energy efficiency, and processing speed of nanocomputing are improving with technological advancements. nanocomputing have not yet reached the level of performance offered by traditional computers, suggesting there is still significant progress needed in this domain.

TABLE 2. Sum & Sqrt

	C1	**C2**	**C3**	**C4**	**C5**	**C6**
M1	100	0.0001	1024	49	4	16
M2	1	0.000001	64	16	1	4
M3	25	0.000025	4096	81	9	25
M4	64	0.000064	16384	36	4	9
SUM	190	0.00019	21568	182	18	54
SQRT	13.78405	0.013784	146.8605	13.49074	4.242641	7.348469

Table 2 presents a comparison of two computational operations, Sum and Square Root (SQRT), using four different nano-computing alternatives. Quantum Dot Nanocomputing offers the highest processing speed of 100 GHz, while DNA Nanocomputing has the lowest processing speed at 1 GHz. The most energy-efficient alternative is DNA Nanocomputing with an energy efficiency of 0.000001, while Quantum Dot Nanocomputing has the highest memory capacity of 1024 gigabytes. For scalability, Molecular Nanocomputing ranks highest with a score of 36, while Carbon Nanotube Nanocomputing displays the highest parallelism at 25. When summing up the performance metrics for all alternatives, the SUM operation scores 190 for processing speed and 0.00019 for energy efficiency, with a memory capacity of 21568 gigabytes. SQRT operation achieves a processing speed of 13.78405 GHz and an energy efficiency of 0.013784, with a memory capacity of 146.8605 gigabytes.

TABLE 3. Normalized Data Matrix

	Normalized Data Matrix					
	C1	**C2**	**C3**	**C4**	**C5**	**C6**
M1	0.725476	0.725476	0.217894	0.518875	0.471405	0.544331

M2	0.072548	0.072548	0.054473	0.2965	0.235702	0.272166
M3	0.362738	0.362738	0.435788	0.667124	0.707107	0.680414
M4	0.580381	0.580381	0.871576	0.44475	0.471405	0.408248

Table 3 presents a Normalized Data Matrix, which represents the relative performance of four nano-computing alternatives in terms of processing speed, energy efficiency, memory capacity, scalability, error rate, and parallelism. The values in the matrix are normalized between 0 and 1, where 1 indicates the highest performance in each category. Among the alternatives, Quantum Dot Nanocomputing shows the highest normalized values for processing speed, energy efficiency, and parallelism, scoring approximately 0.725 in each category. On the other hand, DNA Nanocomputing has the lowest normalized values for all parameters, with scores ranging around 0.072 to 0.297. Carbon Nanotube Nanocomputing and Molecular Nanocomputing fall in between, with normalized scores around 0.363 to 0.871, showcasing their intermediate performance across the evaluated criteria. The matrix provides a comprehensive overview of the normalized performance metrics, allowing for a fair comparison and assessment of the nano-computing alternatives.

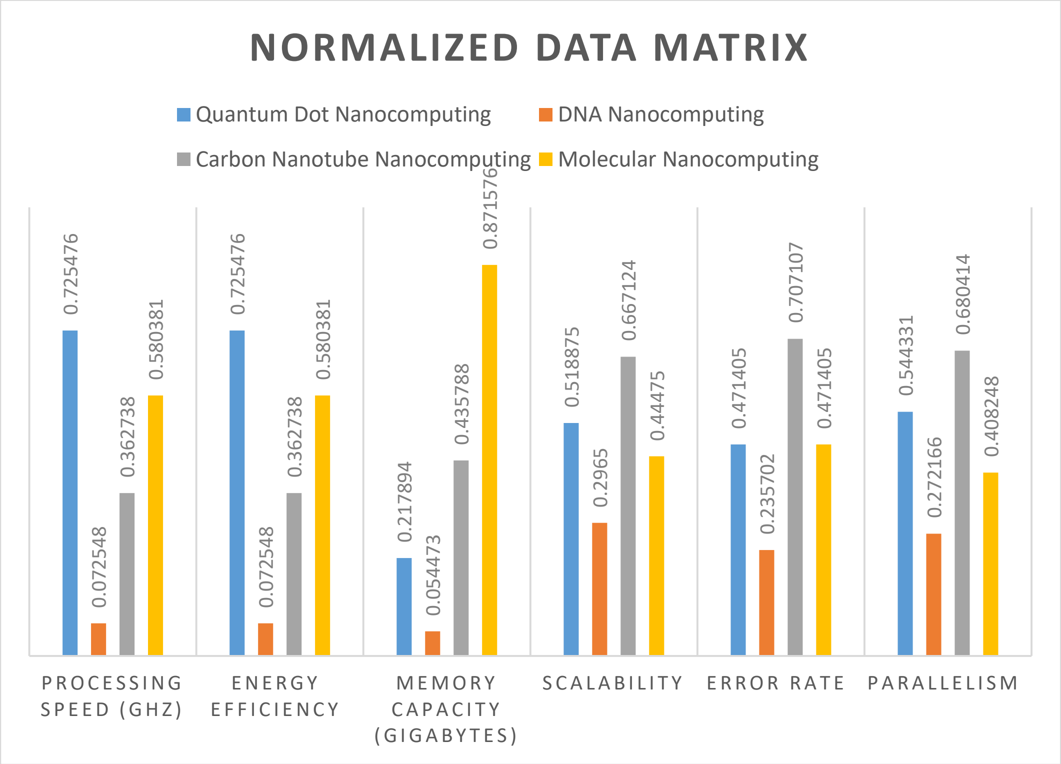

FIGURE 2. Normalized Data Matrix

TABLE 4. Weighted Normalized matrix

Weighted Normalized matrix					
0.2336	0.1652	0.3355	0.1021	0.0424	0.1212
C1	**C2**	**C3**	**C4**	**C5**	**C6**
0.169471	0.119849	0.073103	0.052977	0.019988	0.065973
0.016947	0.011985	0.018276	0.030273	0.009994	0.032986
0.084736	0.059924	0.146207	0.068113	0.029981	0.082466
0.135577	0.095879	0.292414	0.045409	0.019988	0.04948

Table 4 represents the Weighted Normalized Matrix, where each cell corresponds to the weighted and normalized performance of four nano-computing alternatives based on six evaluation criteria: processing speed, energy efficiency, memory capacity, scalability, error rate, and parallelism. The weights assigned to each criterion are indicated in the first row of the matrix. The values in the matrix show the relative importance of each criterion in the decision-making process. For example, the highest weight of 0.3355 is given to memory capacity, indicating its significance in the evaluation. Processing speed and energy efficiency receive weights of 0.2336 and 0.1652, respectively, while scalability, error rate, and parallelism have lower weights of 0.1021, 0.0424, and 0.1212, respectively. The subsequent rows present the normalized performance scores of each alternative, calculated by multiplying the corresponding normalized values from Table 3 with the respective weights. These weighted normalized scores represent the relative performance of each nano-computing alternative in consideration of their importance across all criteria. The Weighted Normalized Matrix facilitates a comprehensive and objective comparison, aiding decision-makers in identifying the most suitable nano-computing alternative based on the specified criteria and their relative importance.

TABLE 5. Concordance Interval Matrix & Discordance Interval Matrix

C12 ={2}	D12 = {1,3,4,5,6}
C13 = {3,5}	D13={1,2,4,6}
C14 = {2}	D14={1,3,4,5,6}
C21={1,3,4,5,6}	D21={2}
C23={1,3,5}	D23={2,4,6}
C24={1,4}	D24={2,3,5,6}
C31={1,2,4,6}	D31={3,5}
C32={2,4,6}	D32={1,3,5}
C34={1,2,4,6}	D34={3,5}
C41={1,3,4,5,6}	D41={2}
C42={2,3,5,6}	D42={1,4}
C43={3,5}	D43={1,2,4,6}

Table 5 displays the Concordance Interval Matrix and Discordance Interval Matrix for four alternatives (C1, C2, C3, and C4). The Cij (Concordance Interval) represents the set of criteria for which alternative Ci is preferred over alternative Cj. Conversely, the Dij (Discordance Interval) shows the set of criteria for which alternative Ci is less favorable than alternative Cj. These matrices help in decision-making by comparing the preferences and disfavor of each alternative against others based on specific criteria.

TABLE 6. Concordance

1	1	1	1	1	1
1	1	0	0	0	0
1	1	0	1	1	1
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	1	1	1	1
1	1	1	1	1	1
0	0	0	1	1	1

Table 6 represents the Concordance Matrix, which is used in multi-criteria decision-making to evaluate the degree of agreement among alternatives based on specific criteria. Each entry in the matrix indicates the concordance level between a pair of alternatives (C1 to C6) for the corresponding criteria. A value of 1 indicates complete concordance, while a value of 0 signifies no concordance. The matrix helps in comparing the preferences and agreements between alternatives across various criteria.

TABLE 7. Concordance Interval Matrix

	Concordance Interval Matrix					c bar
	M1	**M2**	**M3**	**M4**		
M1	0	0.1652	0.3779	0.1652	0.7083	
M2	0.8348	0	0.6115	0.3357	1.782	
M3	0.6221	0.3885	0	0.6221	1.6327	
M4	0.8348	0.6643	0.3779	0	1.877	

	2.2917	1.218	1.3673	1.123	6	0.5

Table 7 presents the Concordance Interval Matrix, which compares the concordance levels between four alternatives (M1, M2, M3, and M4) based on multiple criteria (M1 to M4). Each entry in the matrix represents the degree of concordance between a pair of alternatives for the corresponding criteria. Higher values indicate stronger concordance, while 0 indicates no concordance. The last row displays the sum of concordance values for each alternative, indicating their overall concordance levels across all criteria.

TABLE 8. Concordance Index Matrix

	Concordance Index Matrix			
	M1	**M2**	**M3**	**M4**
M1	0	0	0	0
M2	1	0	1	0
M3	1	0	0	1
M4	1	1	0	0

Table 8 shows the Concordance Index Matrix, which assesses the concordance indices between four alternatives (M1, M2, M3, and M4) based on multiple criteria (M1 to M4). A concordance index of 1 indicates complete concordance, while 0 denotes no concordance. The matrix helps in identifying the level of agreement between alternatives for each criterion.

TABLE 9. Discordance

0	**C1**	**C2**	**C3**	**C4**	**C5**	**C6**
D12	0.152524	0.107864	0.054828	0.022704	0.009994	0.032986
	1					
D13	0.084736	0.059924	0.073103	0.015136	0.009994	0.016493
	1					
D14	0.033894	0.02397	0.21931	0.007568	0	0.016493
	1					
D21	0.152524	0.107864	0.054828	0.022704	0.009994	0.032986
	0.707192					
D23	0.067789	0.047939	0.127931	0.037841	0.019988	0.04948
	0.386769					
D24	0.11863	0.083894	0.274138	0.015136	0.009994	0.016493
	1					
D31	0.084736	0.059924	0.073103	0.015136	0.009994	0.016493
	0.862723					
D32	0.067789	0.047939	0.127931	0.037841	0.019988	0.04948
	1					
D34	0.050841	0.035955	0.146207	0.022704	0.009994	0.032986
	1					
D41	0.033894	0.02397	0.21931	0.007568	0	0.016493
	0.109296					
D42	0.11863	0.083894	0.274138	0.015136	0.009994	0.016493
	0.432738					
D43	0.050841	0.035955	0.146207	0.022704	0.009994	0.032986
	0.347736					

Table 9 represents the Discordance Matrix, which evaluates the discordance values between pairs of criteria (C1 to C6) for each alternative (D12 to D43). The discordance values indicate the level of disagreement between the criteria for each alternative. Higher discordance values signify more significant disagreement, while 0 denotes no discordance. The matrix helps in assessing the level of inconsistency or disagreement among criteria for each alternative.

TABLE 10. Discordance Interval Matrix

Discordance Interval Matrix					
	M1	**M2**	**M3**	**M4**	
M1	0	1	1	1	3
M2	0.707192	0	0.386769	1	2.093961
M3	0.862723	1	0	1	2.862723
M4	0.109296	0.432738	0.347736	0	0.88977
	1.679211	2.432738	1.734505	3	8.846454
				d bar	0.737205

Table 10 displays the Discordance Interval Matrix, which compares the discordance levels between four alternatives (M1, M2, M3, and M4) based on multiple criteria (M1 to M4). Each entry in the matrix indicates the degree of discordance between a pair of alternatives for the corresponding criteria. The last row shows the sum of discordance values for each alternative, denoted as d bar, indicating their overall discordance levels across all criteria.

TABLE 11. Discordance Index matrix

Discordance Index matrix				
	M1	**M2**	**M3**	**M4**
M1	1	0	0	0
M2	1	1	1	0
M3	0	0	1	0
M4	1	1	1	1

Table 11 presents the Discordance Index Matrix, which assesses the discordance indices between four alternatives (M1, M2, M3, and M4) based on multiple criteria (M1 to M4). A discordance index of 1 indicates complete discordance, while 0 denotes no discordance. The matrix helps in identifying the level of disagreement between alternatives for each criterion.

TABLE 12. Net superior value & Rank & Net Inferior Value & Rank

	Net superior value	**Rank**	**Net Inferior Value**	**Rank**
M1	-1.5834	4	1.320789	4
M2	0.564	2	-0.33878	2
M3	0.2654	3	1.128218	3
M4	0.754	1	-2.11023	1

Table 12 presents the Net Superior Value and Rank, as well as the Net Inferior Value and Rank for four nanocomputing alternatives: Quantum Dot Nanocomputing, DNA Nanocomputing, Carbon Nanotube Nanocomputing, and Molecular Nanocomputing. The Net Superior Value represents the overall superiority of each alternative compared to others, while the Net Inferior Value shows their inferiority. Molecular Nanocomputing has the highest Net Superior Value of 0.754, indicating its superior performance compared to other alternatives. It also ranks first in terms of superiority. On the other hand, Quantum Dot Nanocomputing has the lowest Net Superior Value of -1.5834, and it ranks fourth in terms of superiority. Regarding the Net Inferior Value, Molecular Nanocomputing again has the lowest value of -2.11023, highlighting its inferiority compared to others. It also ranks first in terms of inferiority. Conversely, DNA Nanocomputing has the highest Net Inferior Value of -0.33878 and ranks second in terms of inferiority.

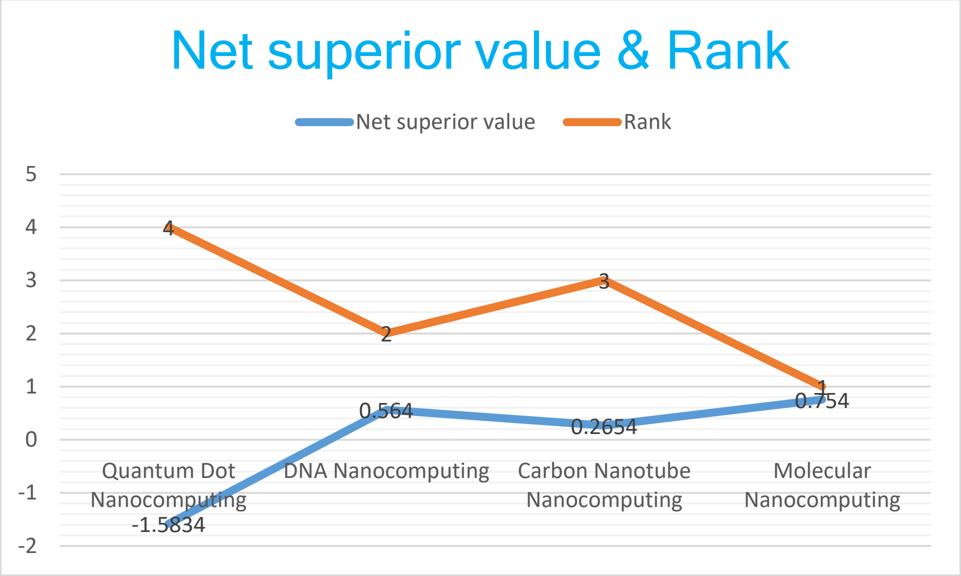

FIGURE 3. Net superior value & Rank

It is a figure 3. showing the net superior value and rank of four different types of nanocomputing: quantum dot nanocomputing, DNA nanocomputing, carbon nanotube nanocomputing, and molecular nanocomputing. The graph shows that quantum dot nanocomputing has the highest net superior value, followed by DNA nanocomputing, carbon nanotube nanocomputing, and molecular nanocomputing. The graph also shows that the rank of the different types of nanocomputing is not always the same as their net superior value. For example, molecular nanocomputing has the lowest net superior value, but it is ranked second. This is because molecular nanocomputing has a very high error rate, which offsets its high parallelism. Overall, the graph shows that there are trade-offs between the different performance metrics for nanocomputing. It is important to choose the type of nanocomputing that is right for the specific application.

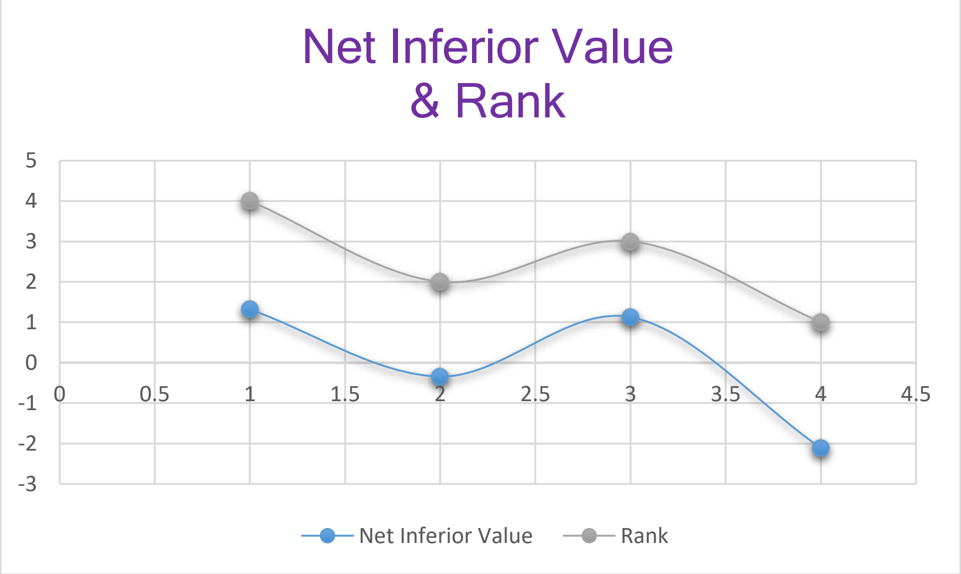

FIGURE 4. Net Inferior Value & Rank

It is a line Figure3. showing the net inferior value and rank of a product. The graph shows that the product has a negative net inferior value, which means that it is inferior to other products in the market. The product is also ranked last, which means that it is the least desirable product in the market. The graph also shows that the net inferior value of the product increases as the rank of the product decreases. This means that the product is becoming more inferior as it falls further down the rankings. Overall, the graph shows that the product is inferior to other products in the market and that it is becoming more inferior as it falls further down the rankings. This suggests that the product may not be successful in the market.

5. CONCLUSION

Nano-computing is a rapidly advancing field that holds tremendous potential for revolutionizing the world of computing. Through the integration of nanomaterials and nanoscale devices, nano-computing seeks to create ultra-small and highly efficient computing systems that can outperform traditional technologies in terms of speed, power consumption, and compactness. The journey of nano-computing has been marked by remarkable progress, paving the way for transformative applications in various industries. nano-computing has the capability to drive significant advancements in diverse fields. One of the key strengths of nano-computing lies in its ability to harness the unique properties of nanoscale materials. Carbon nanotubes, for instance, have attracted substantial attention due to their exceptional mechanical, electronic, and energy properties. Their internal storage capacity through open ends allows for potential integration with other molecular structures, opening doors to innovative memory and computing solutions. Moreover, nano-computing offers an exciting avenue for exploring unconventional computational strategies. By applying basic physical laws directly to the nanocomputing paradigm, researchers can unlock novel computing capabilities that are not achievable using traditional methodologies. This includes the exploration of quantum computing, where nanoscale devices can harness quantum mechanical phenomena to process information in ways that are exponentially more powerful than classical computers. In addition to its potential in processing power, nano-computing presents a promising solution to current limitations in miniaturization. As the demand for smaller and more portable electronic devices grows, nano-computing's compact nature is ideally suited to address these needs, leading to highly integrated and efficient devices with reduced energy consumption. Despite the tremendous potential, challenges remain in nano-computing. The handling of defects and errors in nanoscale manufacturing requires innovative fault-tolerance design methods. Reconfigurable approaches, such as using Bloom filters, have shown promise in addressing these issues, but further research is needed to optimize their stability and error-handling capabilities. nano-computing represents a frontier of technological innovation, with the potential to reshape various industries and improve our quality of life. Continued research and development in this field are crucial to unlocking its full potential and addressing its challenges. As nano-computing evolves, it promises to deliver computing systems that are more powerful, energy-efficient, and compact, paving the way for a new era of computing technology.

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