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Energy-Efficient CMOS and Superconducting Full-Wave Rectifiers

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Abstract: Energy efficiency is a fundamental aspect of modern power conversion systems, aimed at minimizing energy loss and improving overall performance. This paper explores energy-efficient full-wave rectifiers, focusing on two key technologies: CMOS and superconducting materials. Energy-efficient CMOS rectifiers are widely used in low-power applications due to their ability to operate with minimal power consumption and their compatibility with integrated circuit technologies. The paper discusses recent advancements in CMOS rectifier designs, highlighting innovations that enhance efficiency while reducing energy dissipation. In addition, superconducting full-wave rectifiers are examined for their exceptional energy efficiency, driven by their ability to operate with almost no power loss and reduced thermal noise. Superconducting materials offer significant advantages, especially in ultra-low power applications and energy-harvesting systems, where maintaining minimal energy consumption is crucial. The paper concludes by exploring the potential of CMOS and superconducting rectifiers to contribute to the development of more energy-efficient power conversion systems and their relevance to various low-power and energy-efficient applications.

Keywords: Full wave rectifiers, converters, voltage conveyers, harmonic distortion.

1. INTRODUCTION

Currently, the rapid expansion of technological applications plays a crucial role across multiple sectors, directly impacting the effectiveness and performance of developed components. The Schottky diode, created through the metal-semiconductor interface, is deemed ideal for high-frequency applications. The field of semiconductor electronics primarily relies on metal-semiconductor junctions, which are extensively utilized in microelectronics, including diodes. A diode's efficiency increases when the reverse voltage it can withstand in the blocked state is higher, when its forward voltage drop in the on state is minimal, and when its switching times are reduced. Since fulfilling all three conditions simultaneously is not feasible, the selection of a diode must be based on the specific application it is designed for [3].

Diodes play a crucial role in power control and distribution in modern integrated circuits. Therefore, superconducting diodes are expected to be essential for efficient, compact bias-handling systems in cryogenic electronics and detectors. The primary function of superconducting diodes would involve AC-to-DC conversion at low temperatures (for example, through full-wave bridge rectifiers) to deliver stable and tunable DC bias currents using RF signals. This process could be beneficial for transmitting power from room temperature with a minimal number of RF lines or for linking different subsystems within the same cryogenic setup. Superconducting diodes could also perform other common diode functions, such as frequency mixing, signal modulation, voltage-controlled oscillation, and isolation, contributing to the advancement of various cryogenic platforms.

Currently, multilevel converters [5–6] are being studied by many researchers, which control through a specific circuit topology the output terminals of different DC power supplies connected in series. By changing the switching states of the circuit, a multi-step wave can be made equivalent to a sine wave. Compared to traditional two-level converters, several advantages are offered by multilevel converters: 1) Reduced voltage stress on semiconductor switching devices, allowing for higher voltage and power output; 2) High output power quality, with low dv/dt, reduced total harmonic distortion (THD), and minimized electromagnetic interference; 3) Operation at both the fundamental wave and high switching frequencies, which reduces switching losses and improves system efficiency. These benefits have led to the widespread use of multilevel rectifiers in power supply

systems, power factor correction, battery energy storage systems, and other applications [7]. However, some shortcomings remain for multilevel converters. One of these is the exponential increase in the number of switching devices as the level numbers rise, complicating the control strategy and increasing system costs, as each switch requires its own gate driving circuit [9]. Researchers continue to innovate and improve multilevel topology in pursuit of better performance.

Diodes in this section function according to their operating conditions, such as voltage, frequency, and current, making it essential to study each diode's characteristics in order to enhance performance and reduce energy losses in the circuit [4]. High-voltage diodes, which are designed to achieve high blocking voltage, require the N-- region to be significantly thickened, typically around 100μm per hundreds of volts. This increases both the forward voltage drop and the stored charge [5]. Conversely, controlled avalanche diodes are engineered to withstand the avalanche effect without sustaining damage during brief but repetitive intervals, with characteristics such as reverse breakdown voltage and reverse current corresponding to maximum power dissipation. Furthermore, fast diodes intended for high-frequency operations must feature a minimal residual stored charge (QR), as switching losses are directly related to QR. To minimize QR, the lifetime of minority carriers in the N-- region is reduced, encouraging recombination during the decay of forward current. Schottky diodes, for instance, exhibit low forward voltage drops. In PN junction diodes, the forward voltage drop is influenced by the resistivity of the N-- region, which decreases as doping increases. The epitaxial junction allows for a precise control of doping in each layer, thus reducing the voltage drop to less than 1 volt for nominal current [7,8].

2. LITERATURE REVIEW

The ability to process both voltage and current signals is a remarkable feature, made possible by the presence of output ports with appropriate impedances for both voltage and current signals. The configuration involves two voltage conveyors (VCs), two diodes, and one resistor. A full-wave rectifier (FWR) with suitable output impedance for the voltage signal is presented in [14], where a second-generation voltage conveyor (VCII) is used along with two diodes and two resistors. In some configurations, two FWRs operating in current-mode are explored: one utilizes a single operational transconductance amplifier (OTA), two diodes, and two resistors, while the other incorporates a differential voltage current conveyor (DVCC), two diodes, and three resistors. Additionally, another design featuring DVCCs as active components is presented, consisting of two DVCCs, two resistors, and two diodes. The current-mode circuit supports cascadability due to the presence of proper input and output impedances. The precision rectifier reported in [17] works in voltage-mode, employing three current feedback operational amplifiers (CFOAs), two resistors, and one MOS switch, with appropriate impedances at both input and output.

Recently, coupling between ferroelectricity and superconductivity was observed in bilayer MoTe2 [88] while simultaneous ferromagnetism and electric polarity were seen for the first time in a metal, (Fe0.5Co0.5)5GeTe2 [89], raising prospects of intrinsic or proximity-induced superconductivity in it to create a SD that is robustly trainable by both electric and magnetic fields. Along with the logic and designs described in this work, the above developments lay the groundwork and motivate a search for platforms for superconducting digital electronics.

Energy-efficient full-wave rectifiers are integral to applications in energy harvesting and advanced electronics. CMOS-based designs have gained traction due to their scalability and compatibility with commercial applications. **Ali et al. (2023)** introduced a 13.56 MHz single-stage CMOS voltage-boosting rectifier tailored for biomedical implants. Their design achieved a PCE of 98.2% and a VCR of 120%, demonstrating its efficacy in low-power medical devices (Ali et al., 2023). Similarly, **Chang et al. (2023)** proposed a CMOS rectifier with internal threshold voltage compensation, achieving 86% efficiency in wireless power receivers. This approach effectively addressed power losses caused by threshold voltages in diodes (Chang et al., 2023). **Sharma et al. (2020)** designed a high-efficiency RF-DC CMOS rectifier for RF energy harvesting, showcasing its application in IoT devices requiring low input power (Sharma et al., 2020).

On the other hand, superconducting rectifiers have been explored for niche, high-performance applications. **Kumar et al. (2024)** developed a superconducting diode using niobium nitride, achieving 43% rectification efficiency under cryogenic conditions. Their work emphasized applications in quantum circuits requiring AC-to-DC conversion (Kumar et al., 2024). **Lee et al. (2024)** introduced gate-controlled superconducting switches, demonstrating their potential in cryogenic environments with dynamically tunable characteristics for signal rectification (Lee et al., 2024). Additionally, **Singh et al. (2024)** integrated superconducting diodes with logic gates for low-temperature electronics, enabling efficient signal processing in quantum systems (Singh et al., 2024).

3. RESEARCH METHODOLOGY

The research methodology focuses on evaluating energy-efficient designs of CMOS and superconducting full-wave rectifiers. Initially, a comprehensive literature review is conducted to understand current designs, limitations, and key efficiency parameters. Analytical modeling is employed to derive theoretical frameworks for power conversion efficiency, signal integrity, and thermal performance. Simulation-based validation is carried out using advanced EDA tools to compare CMOS and superconducting rectifiers under various operating conditions. Prototype designs are developed for experimental testing to verify simulation results and measure real-world performance metrics, including power loss, conversion efficiency, and temperature management. Statistical analysis is applied to interpret results and ensure reliability. Comparative studies highlight trade-offs in terms of energy efficiency, scalability, and cost-effectiveness. Findings are benchmarked against industry standards to assess practical viability. This methodology ensures a robust evaluation framework for advancing energy-efficient rectifier designs.

Bridge rectifier with vortex diodes

Our vortex diodes were 1 µm wide wires patterned on NbN films with three different thicknesses (9 nm, 13 nm, and 14 nm), deposited on a 300 nm thick thermal-silicon-oxide (SiO2) on silicon substrate. Figure 1a shows the scanning electron micrograph of the device and an illustration of the operating principle. The triangular notch lowers the vortex surface barrier on the left side due to current crowding, 39 while the barrier on the right edge remains unchanged. A current $I+$ generates a Lorentz force that pushes vortices towards the center of the wire. When this force is large enough, vortices cross the wire from the lower barrier on the left, generating a hotspot (resistive state). When an out-of-plane magnetic field is applied, a screening current circulates at the edges of the wire (Meissner effect). Since this Meissner current flows in opposite directions on the two edges, the surface barrier of one edge.

Rectification efficiency

The rectification efficiency $\eta = \frac{|I_c^+| - |I_c^-|}{|I_c^+| + |I_c^-|}$ is a critical figure of merit to be maximized for optimal rectification. We measured the I-V characteristic of the diodes to extract the positive and negative critical currents ($Ic+$ and $Ic-$ respectively). Figure 2a shows the I-V curves of a diode patterned on the 14 nm thick film, for different values of the field. With positive magnetic fields (entering the plane) the negative critical current $|Ic-|$ increased, and the positive critical current $|Ic+|$ decreased. Negative magnetic fields caused the opposite effect. We studied how the critical currents and rectification efficiency vary with the magnetic field by applying a 1 kHz triangular wave to a device shunted with 1 MΩ. The upper panel of figure 2b shows that $|Ic+|$ and $|Ic-|$ were equal at zero magnetic field. $|Ic-|$ linearly increased with an increasing positive field up to a peak value, while $|Ic+|$ decreased. After the peak, $|Ic-|$ linearly decreased because the surface barrier on the right edge became smaller than the barrier on the left. At about ±5.5 mT, the relation ceased to be linear and both negative and positive currents approached similar low values because bulk vortex pinning effects dominated.38 The peak of $|Ic-|$ was higher than the peak of $|Ic+|$, as observed by Suri et al. 38

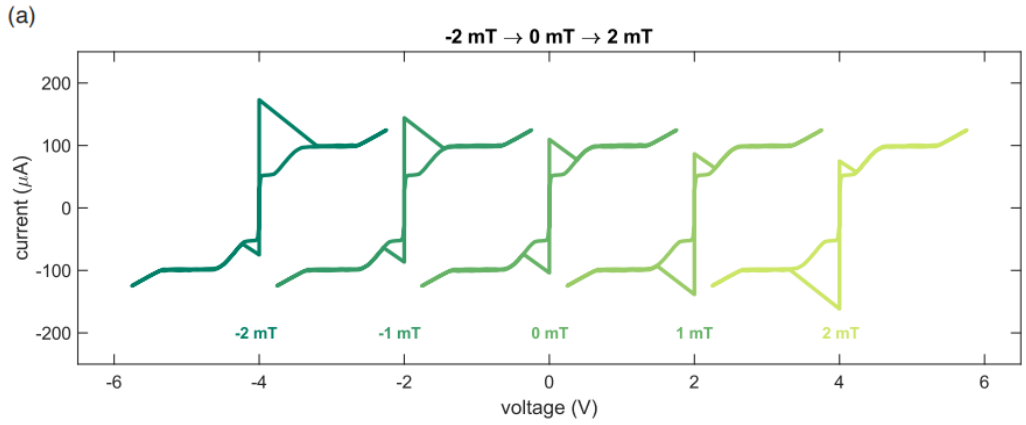

FIGURE 1. a shows the I-V curves

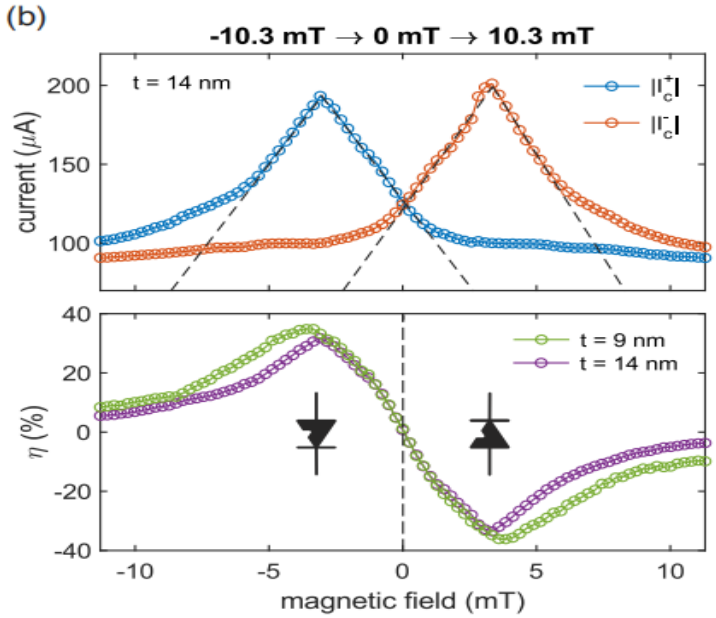

FIGURE 2.

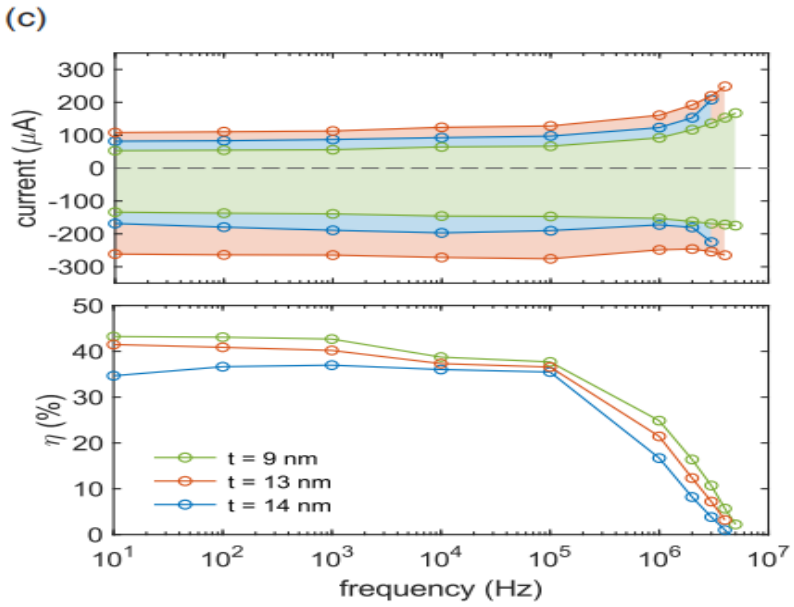

FIGURE 3.

AC-to-DC conversion: The device could rectify continuous sinusoidal signals up to 3 MHz. However, we observed rectification at higher frequencies in burst mode. Figure 4a shows a fully rectified 50 MHz sinusoidal signal applied for 100 ns with a 1 µs burst period. At this frequency, a longer burst duration caused instability in the system (only a portion of semi-periods were rectified after 100 µs). We believe the observed difference in maximum operating frequency between the continuous and burst modes was due to the system heating up significantly during the continuous operation, while having time to cool off between bursts in burst mode.Figure 4: Operating the bridge rectifier and AC-to-DC converter at 50 MHz. (a) Full-wave rectification of a sinusoidal signal for 100 ns. The input signal *i*IN is set to burst mode with a 1 µs burst period. The load *R*L is 50 Ω (100 Ω surface-mount resistor in parallel with the 100 Ω differential mode impedance from the amplifiers). There is a transient for the lower level of the output signal *i*OUT because the input capacitance of the used amplifiers need to be charged. (b) AC-to-DC conversion with a 500 pF smoothing capacitor (see figure 1c), for 440 ns in burst mode (the burst period is 100 µs). The red dashed line indicates the value of the output DC current (69 µA) between 340 ns and 520 ns.

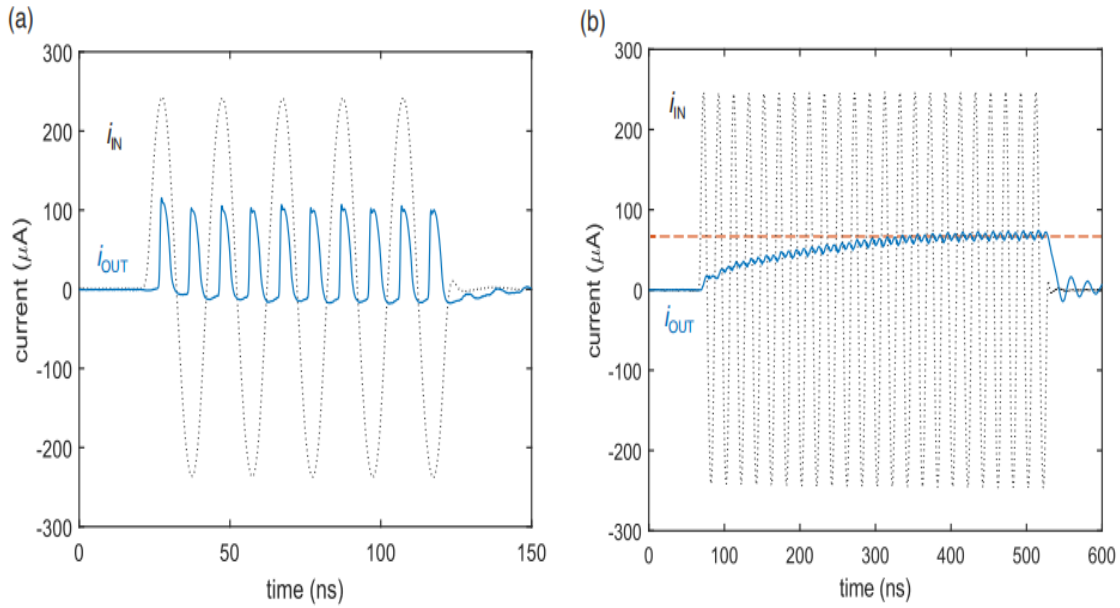

FIGURE 4A shows a fully rectified 50 MHz, **FIGURE 4B** shows the output current of the converter through the load resistor

Considering that the circuit could operate up to 50 MHz in burst mode, we demonstrated AC-to-DC conversion by shunting the load *R*L with a 500 pF surface-mount smoothing capacitor . Figure 4b shows the output current of the converter through the load resistor. The device could operate for a 460 ns long burst (burst period: 100 µs), with an 8% ripple whose amplitude was set by the capacitance. The DC value of the current saturated to 69 µA. The waveform in the figure was averaged over 100 signals to increase the SNR and thus extract the ripple amplitude. A single trace without averaging is shown in the supplementary material. After a start-up time of about 300 ns, the capacitor was correctly charged at each semi-period, for all the acquired signals. It is worth mentioning that including the smoothing capacitor enabled correct rectification for a longer burst duration compared to the configuration with a resistive load. This difference likely comes from the intrinsic dependence on load impedance for the hotspot growth and, consequently, for thermal dissipation.

Full-wave rectification: experiment and simulation

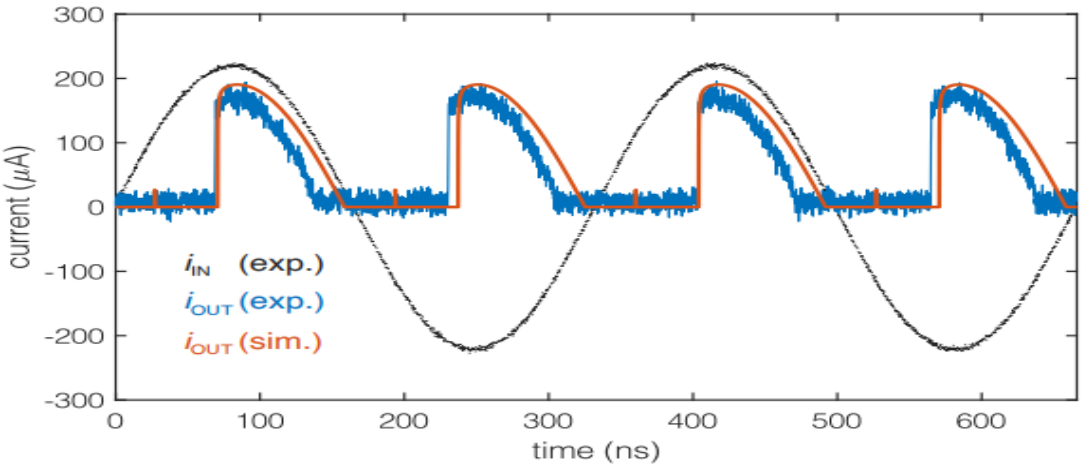

FIGURE 5. shows the comparison between the experimental and simulated full-wave rectification

Figure 5 shows the comparison between the experimental and simulated full-wave rectification of a continuous sinusoidal signal at 3 MHz. The simulation was performed on the bridge rectifier with *LR*/*L*L = 10, using the LTspice model described in the Methods section. In the simulated output, the fast rising edge, which corresponds to the switch of twoFigure S4: Comparison between experimental and simulated full-wave rectification at 3 MHz.

The black trace is the experimental input current of the rectifier. The blue trace is the experimental output current without averaging. The red trace is the output current simulated with the parameters listed in the Methods section. diodes in the rectifier, always happens at the same time for each semi-period. In the experimental trace, the switch happens at different times for each semi-period, due to noise and thermal fluctuations in the devices.

In the experiment, the peak output current is slightly lower than in simulations. Moreover, the experimental output signal drops to zero for a lower input current than in simulations. This difference might be explained by the retrapping current of the diode being higher than in the LTspice model.

However, the effect should equally modify the margins also in the experimental I-V curves but we did not observe it. Therefore, further characterization of the circuit is required to fully understand this problem. In simulations, the effect disappears at higher frequencies (e.g. at 50 MHz) because the input current increases fast enough to sustain a hotspot when *D*2 or *D*3 switch.

4. RESULT AND DISCUSSION

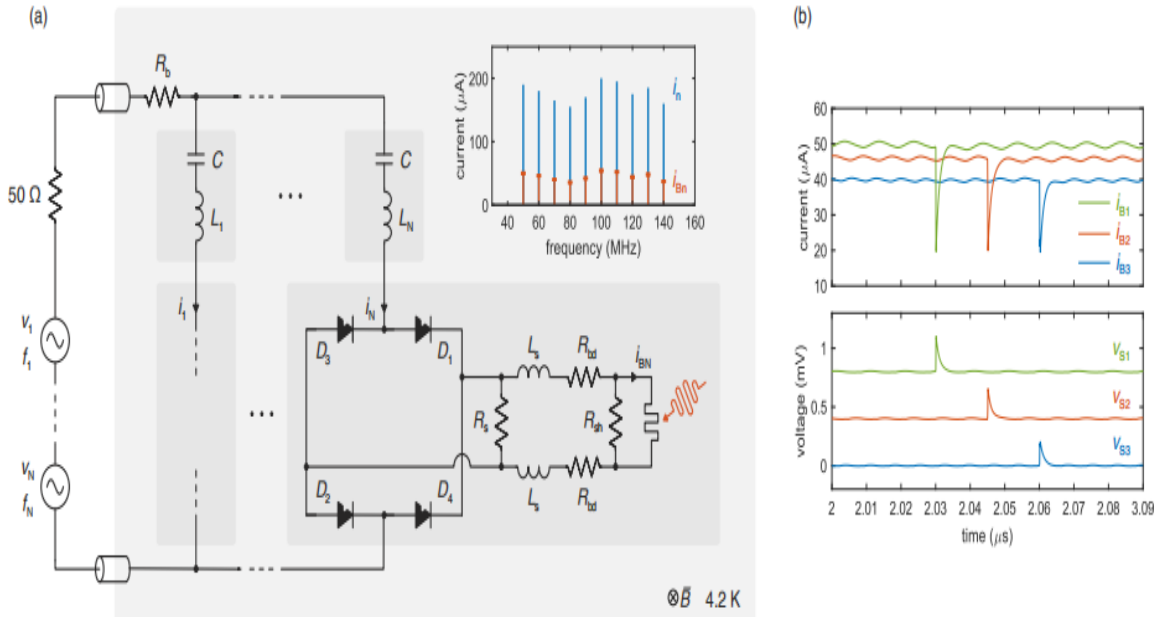

FIGURE 6. Design and simulation of a bias distribution network

Figure 6: Design and simulation of a bias distribution network based on superconducting bridge rectifiers. (a) Circuit schematic of a network to bias *N* SNSPDs. All the components in the gray box are placed at 4.2 K, and the field is applied to the entire system. The voltage source at room temperature generates *N* sinusoidal signals (*v*n) at *N* different frequencies (*f*n). Each signal couples to a specific superconducting LC series resonator (*C* and *L*n). The resonators are connected in parallel. Each resonator is in series with a bridge rectifier, which drives an inductive low-pass filter. The filter generates a DC current passing through a shunted SNSPD. The upper-right inset shows the distribution of different bias levels for *N* = 10. The amplitude of the AC input current *i*n of each rectifier is in blue. The DC current through the SNSPD, with associated ripple (error bars), is in red. (b) Simulated time-domain behavior for three SNSPDs (respectively coupled to signals at 50 MHz, 60 MHz, 70 MHz) switching at different times in the network of ten SNSPDs. Upper panel: current through the SNSPDs. lower panel: voltage *v*Sn across the shunt resistor *R*sh of the SNSPDs. Traces in the lower panel are vertically shifted for clarity. Circuit parameters: *I*c + = 100 μA, *I*c − = 200 μA, *R*b = 45 Ω, *C* = 1 pF, *R*s = 5 Ω, *L*s = 250 nH, *R*sh = 10 Ω, *R*bd = 2.5 Ω, SNSPD inductance: *L*d = 10 nH.

5. CONCLUSION

The designed architecture would have a relatively large footprint when implemented. The area of each module would be dominated by the capacitor *C* and the inductor *L*n. If rectifiers operating at higher frequencies were demonstrated, the footprint of the resonators could be decreased. Otherwise, a multi-layer fabrication process

might be used to minimize the occupied area. In particular, parallel-plate capacitors could be used. Moreover, a normal metal layer should be included for the integrated resitors. Another circuit element that largely contributes to the occupied area is the large inductor in the low-pass filter. Its inductance can be in principle reduced, however, the ripple on the output current would increase.

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