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Designing an Improved Intellectual Property Core Using Image Processing for Hetrogenous Architecture

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Abstract: *The rapid evolution of heterogeneous computing demands optimized Intellectual Property (IP) cores for enhanced performance. This paper presents an improved IP core leveraging image processing techniques to optimize computational efficiency. The proposed design enhances processing speed and minimizes latency by utilizing parallelism and hardware acceleration. It integrates adaptive processing mechanisms and efficient data handling strategies. Optimized memory management further improves resource utilization and power efficiency. The architecture ensures scalability and seamless integration within heterogeneous environments. Performance evaluation demonstrates a significant reduction in computation time. Comparative analysis highlights superior efficiency over conventional IP cores. The design is tailored for real-time image processing applications. Hardware acceleration techniques improve processing throughput. The proposed approach ensures dynamic adaptability across diverse computing platforms. Implementation feasibility is validated through experimental results. Resource-efficient computation supports energy-conscious design goals. The improved IP core contributes to next-generation high-performance computing systems. This work advances IP core development for modern heterogeneous architectures.*

Keywords*: Deep Learning, Fully Convolutional Networks, Image Processing, Intellectual Property.*

1. INTRODUCTION

The advancement of semiconductor techniques, computers and electronic technology has led to a constant improvement in the computational efficiency and feature-richness of integrated digital image processing systems. Embedded computerised image processing is a current area of study both domestically and abroad. It has been widely used in a number of engineering disciplines, mainly digital communications, industrial manufacturing, biomedical science, remote sensing image processing, exploration of space, and the prediction of weather. The main components of conventional digital image processing devices are image processing software, computers for general use, and picture acquisition cards. In embedded image processing applications, it is challenging to achieve the system specifications for size, power usage, and cost due to their performance limitations imposed by the CPU design, computer bus, and printed circuit architecture. Integrated techniques for image processing systems that meet technical requirements for volume and power consumption have been made possible by the development of processors that are embedded (DSPs, ARMs, etc.). However, they don't meet the computer needs for performance.

An ISP improves image quality by carrying out several processing jobs like reduction of noise, sharpness, improvement, and colour restoration. It is made up of a number of image processing devices coupled in a pipeline structure. The performance of the classic ISP is dependable, constant, and predictable when each submodule's actions and settings are typically fixed. However, it struggles to handle complicated scenes with varying lighting circumstances [1], and it takes a lot of fine-tuning on the requirements and pipeline composition to achieve decent imaging results. Despite significant advancements in dehazing, denoising, and other areas of image processing using conventional techniques [2,3], the aforementioned issues remain unresolved. However, it's evident that the ease and supremacy of image processing using neural networks has spurred more talks at conferences and in publications.

As deep learning has advanced in recent years, an increasing amount of research has tried to employ deep learning techniques to imitate the full classical ISP pipeline or to enhance the quality of images in a specific dimension

[4]. A precedent for the use of neural networks in image segmentation was established with the introduction of Fully Convolutional Networks (FCN) and UNet, which significantly decreased the quantity of data needed for training deep learning neural networks, which needed thousands of data with annotations. As a result, algorithms for solving from beginning to end Super-Resolution (SR) issues have been developed. These include SRGAN utilising generative adversarial systems VDSR with a ResNet structure, and SRCNN (the first try to figure out SR difficulties using a CNN structure). Prior to the 2018 work "Learning to See in the Dark," which employed UNet to address the imaging challenge in low-light conditions, the aforementioned research was all focused on deep learning techniques determined by a single problem. Implementing RGB as the output and RAW Bayer as the input, the model was a full ISP from an imaging standpoint and started a trend of using a single deep learning model to replace entire ISP pipeline operations.

The researchers proposed a novel pyramid CNN's construction for fine-grained restoration of images called PyNet [5], a full throughout its entirety deep neural model called DeepISP, and CycleISP, that accomplished the highest level of accuracy on real camera comparable datasets [6] in 2020, to handle becoming more complicated environments and improve imaging results. The channel spatial attention approach is used in both CSANet [7] and PyNET-CA [8], two more recent and intriguing investigations. Typically, Deep Learning ISP (DLISP) refers to a group of deep learning-implemented image processing units, including DeepISP, PyNet, CycleISP, and CSANet. However, DLISP does not require the organisation of permanent pipelines and manual variable adjustments, nor does it include predefined submodules to perform various operations. Instead, it frequently uses a single end-to-end neural network (such a fully convolutional neural network like UNet or WNet) to imitate the processing impacts of the complete ISP network.

DLISP offers better processing performance in some situations and is more flexible as it can obtain multidimensional and complicated features from vast volumes of focused training sets [9]. Additionally, the model may be optimised and iterated more easily without requiring a lot of manual labour. But DLISP needs a lot of processing power and storage space. The majority of research focusses on enhancing the output image quality, but it ignores the high real-time needs and constrained computational resources that make it difficult to replicate these results. The shortage of equipment computing power implies that just a few DLISP models can be successfully applied for production and used in real-time scenarios, despite the fact that researchers in academia and industry have suggested numerous DLISP models that frequently outperform conventional ISP pipelines in challenging conditions like low light and high noise. Highly effective CPU and GPU clusters cannot be integrated to derive neural networks for real-time processing, particularly in edge settings. Consequently, specialised hardware acceleration approaches for deep learning edge interpretation are required to allow deep learning to play a more rational role and generate greater value in real-world circumstances. DLISP and classical approaches have been tried together, but nobody has been able to sufficiently clarify how image processing jobs should be divided, why this division should be made, or the manner in which to more efficiently combine the two to effectively utilise their respective advantages.

2. LITERATURE REVIEW

Shafi et al., have suggested the computational constraints of the edge devices, which lead to inadequate inference speed and prohibit them from fulfilling the most fundamental need of immediate performance as an ISP, are the true barrier to the standardisation and production deployment of the present DLISPs. In order to accelerate neural network learning in edge conditions, accelerators must be designed. In edge circumstances, the most common method for speeding up neural network inference is to create specialised hardware accelerators like NVDLA and other NPUs [10]. Zhou et al., have stated that in addition to having a lengthy development cycle and a high architectural difficulty, hardware accelerations with broad architectures performed through ASICs would not be adequate for satisfying the real-time requirements with regard to of accelerating ratio. Furthermore, in order to schedule, general-purpose NPUs frequently need software, and the CPU might require to execute an operating system. This makes development more challenging and prolongs memory access times. In order to increase the inference speed of particular operators, some researchers have suggested strategies that optimise hardware architectures for particular models, eliminating duplicate topologies and consolidating hardware resources [11,12,13]. However, this method simply lessens the NPU's universality and adaptability which renders implementing it more challenging.

Baldeon et al., have provided a contemporary application in medical image processing involves deep learning, particularly in medical segmentation. Traditional approaches rely on manually designed neural networks for segmentation, requiring extensive training time and large datasets. To address this, the exploration of multi-objective Neural Architecture Search (NAS) has been introduced, enabling the automated creation of accurate and

efficient segmentation architectures. Within this context, EMONAS-Net is proposed as a multi-objective NAS framework specifically developed for 3D medical image segmentation. The segmentation process is adapted based on network size, incorporating two key components: a structural configuration at both the micro and macro levels and an algorithm driven by multi-objective evolution assisted by surrogates. This algorithm, SaMEA, enhances hyperparameter optimization by identifying subproblems early in the evolutionary process, improving mutation performance and accelerating convergence. Additionally, a Random Forest-based surrogate model is integrated to expedite fitness evaluation of architectures. EMONAS-Net has been evaluated in multiple segmentation challenges, including prostate segmentation in the MICCAI PROMISE challenge, hippocampal segmentation in the Medical Segmentation Decathlon challenge, and cardiac segmentation in the MICCAI ACDC challenge. The proposed framework demonstrated superior performance compared to existing NAS methods, achieving a 50% reduction in search time while maintaining a more compact design [14].

Wang et al., have stated that artificial intelligence systems involve the examination of deep neural frameworks, though they encounter specific challenges. To address these, a Dynamic Neural Architecture Refinement (DNAR) model is introduced, aimed at improving the configuration of Convolutional Neural Networks (CNNs) through modular neural components. This approach utilizes discrete propagation within the refinement process to enhance both model precision and the rate of convergence. Design constraints are imposed to regulate CNN structural parameters, and a specialized function is devised to balance accuracy with the progression of training convergence. The neural framework is employed to assess system effectiveness in refining optimization efficiency, utilizing a heuristic strategy to advance the enhancement process. The DNAR model has been implemented for detecting retinal conditions, where eight CNN variants were analysed and benchmarked against DNAR in terms of precision and convergence behaviour. The findings revealed outstanding effectiveness, demonstrating that this model can be seamlessly integrated into CNN structures for diverse datasets [15].

Zhou et al., have proposed a medical image processing, that often employs semi-supervised classification and segmentation techniques, which have been widely studied. These approaches can enhance the efficiency of fully supervised models by incorporating additional unlabeled data. To leverage this advantage, a Semi-Supervised Medical Image Detector (SSMD) is proposed. SSMD aims to enable supervision-free learning by effectively utilizing unlabeled data while ensuring stable and reliable predictions. To achieve this, an adaptive coherence cost function is implemented to regulate different prediction components. Furthermore, various perturbation techniques are applied to maintain consistency across feature spaces, including image representations, allowing the detector to generate accurate and dependable results. Extensive experimental evaluations of SSMD across multiple settings have demonstrated its resilience and effectiveness [16].

3. RESEARCH METHODOLOGY

To develop an optimized IP core for high-performance heterogeneous computing, an in-depth analysis of existing IP cores was conducted to identify inefficiencies in computational speed, latency, and resource utilization. Image processing techniques were incorporated to enhance parallelism and leverage hardware acceleration. The design integrates adaptive processing mechanisms and efficient data handling strategies to optimize performance. Memory management techniques were refined to improve resource allocation and energy efficiency. Implementation and testing were carried out across diverse computing environments to ensure scalability and seamless integration. Performance evaluation involved experimental analysis of computation time, processing throughput, and power efficiency. A comparative assessment against conventional IP cores validated the improvements in speed and resource utilization. The final design was evaluated for real-time image processing applications, confirming its feasibility for next-generation heterogeneous computing systems.

Evolution of Digital Image Processing Systems: The development of electronic technology, computer systems, and semiconductor processes has led to significant changes in digital image processing systems. These changes include improvements in system composition, technical specifications, design methods, and tools. Embedded applications have grown alongside digital image processing, benefiting from these advancements. The development of digital image processing systems can be divided into three stages. The first stage (1960s–1980s) saw the introduction of image computers and analysis systems in the United States and the United Kingdom. These systems were large, expensive, and highly functional, using a chassis-based structure. In China, Tsinghua University developed similar image processing and acquisition systems, following the same design approach. During the second stage (1980s–1990s), image processing systems became smaller and more efficient. They used plug-in cards combined with computers to create image acquisition systems. In China, Tsinghua University and the Chinese Academy of Sciences developed image acquisition cards that were affordable, compact, and easy to

use, making them widely adopted. These systems used large-scale integrated circuits, with PCs as the primary platform and the ISA bus as the standard interface. The third stage (1990s–present) introduced two main types of image processing systems. The first type continued using plug-in cards, with the PCI bus gradually replacing the older ISA interface. Many Chinese companies produced PCI-based image acquisition cards, allowing image processing through Windows-based software. The second type adopted embedded solutions, using Digital Signal Processors (DSPs), Field-Programmable Gate Arrays (FPGAs), and Application-Specific Integrated Circuits (ASICs). These cost-effective chips became essential components of embedded image processing systems. Since the early 21st century, ARM, DSP, and FPGA-based image processing systems have advanced significantly. Compared to PC-based platforms, embedded systems offer advantages such as smaller size, lower cost, better performance, and simpler structures. Research shows that FPGA-based embedded systems excel in computational efficiency, but practical applications may face challenges related to system structure and cost. The Zynq-7000 SoC, which combines an ARM processor with FPGA technology, helps overcome these challenges by integrating processing and programmable logic.

Role of Image Processing in Intellectual Property (IP) Core Design: Image processing plays a critical role in the design and optimization of Intellectual Property (IP) cores, particularly in heterogeneous architectures where computational efficiency and resource utilization are paramount. IP cores dedicated to image processing are designed to perform complex tasks such as feature extraction, image enhancement, object detection, and compression while ensuring optimal performance in real-time applications. These cores are widely used in domains such as computer vision, medical imaging, remote sensing, and industrial automation, where accurate and efficient image processing is essential. One of the primary functions of image processing in IP core design is feature extraction, where key characteristics such as edges, textures, and patterns are identified for further analysis. This is crucial in applications like biometric authentication, where fingerprints or facial features need to be accurately processed. Additionally, compression and optimization techniques such as JPEG and wavelet-based encoding reduce the data size without significant loss of quality, enabling efficient storage and transmission in bandwidth-constrained environments. Edge detection and segmentation methods, including Sobel, Canny, and thresholding techniques, enhance image clarity and improve pattern recognition, making them suitable for industrial quality control and surveillance applications.

The integration of image processing in IP cores is further enhanced through hardware acceleration using FPGA, GPU, or ASIC implementations. These architectures facilitate parallel processing, enabling high-speed computations and reduced latency, which are critical in real-time systems. The use of heterogeneous architectures allows efficient task allocation, where computationally intensive image processing operations can be offloaded to specialized hardware, while control and decision-making functions are managed by general-purpose processors. This approach not only improves processing speed but also enhances power efficiency, making it ideal for embedded systems and edge computing applications.

Key Image Processing Techniques for IP Core Optimization: Optimizing an Intellectual Property (IP) core for image processing in a heterogeneous architecture requires the implementation of efficient image processing techniques that enhance performance, reduce computational complexity, and improve resource utilization. These techniques ensure that the IP core operates efficiently while handling large volumes of image data in real-time applications. Some of the key techniques for IP core optimization include preprocessing, transformation, object recognition, and parallel processing.

Transformations for Efficient Data Representation: Transformations convert image data into different domains to simplify processing. The Fast Fourier Transform (FFT) enables efficient filtering in the frequency domain, while the Discrete Wavelet Transform (DWT) provides multi-resolution representation for compression and feature extraction. Principal Component Analysis (PCA) reduces data dimensionality while preserving essential features, optimizing storage and improving classification accuracy.

Feature Extraction and Object Recognition: Efficient feature extraction and object recognition improve processing speed by focusing computational resources on relevant image regions. Edge detection methods like Sobel, Prewitt, and Canny highlight object boundaries, aiding segmentation. Histogram-based thresholding helps identify key regions based on pixel intensity distribution, while template matching compares image sections with predefined patterns for accurate object detection.

Parallel Processing for Performance Optimization: Parallel processing enhances computational efficiency by distributing workloads across CPUs, GPUs, and FPGAs. FPGA-based acceleration reduces latency by

implementing real-time image processing in hardware, while GPUs leverage their parallel architecture for high-speed convolution and matrix operations. Hybrid CPU-GPU processing dynamically allocates tasks, optimizing both performance and energy efficiency. These techniques collectively enhance the efficiency of IP cores, enabling real-time image processing with optimized resource utilization and computational performance. Let me know if you need further refinements.

Energy-Efficient Design Considerations: Energy efficiency is a key aspect of designing an effective IP core, as power consumption directly influences the performance and sustainability of embedded systems, especially in resource-constrained environments. Dynamic Voltage and Frequency Scaling (DVFS) is implemented to adjust power consumption based on workload demands, reducing energy wastage. Clock gating minimizes power usage by selectively disabling idle functional units, while efficient memory access patterns help reduce redundant data transfers, optimizing cache utilization and improving energy efficiency. These design considerations ensure that the proposed IP core maintains a balance between high performance and low power consumption.

Heterogeneous Architectures: Heterogeneous architectures integrate multiple types of processing units, such as CPUs, GPUs, FPGAs, and ASICs, within a single system. These architectures enhance computational efficiency by leveraging the strengths of different processing elements. CPUs handle general-purpose tasks, while GPUs accelerate parallel computations, and FPGAs or ASICs provide specialized processing capabilities. This approach optimizes performance, power consumption, and flexibility in executing diverse workloads. Heterogeneous architectures are widely used in artificial intelligence, image processing, cloud computing, and embedded systems. By distributing tasks among specialized hardware, they improve execution speed and resource utilization. These architectures enable real-time processing of large datasets and complex algorithms. High-performance computing benefits from their ability to handle intensive parallel operations efficiently. They also support energy-efficient processing by offloading tasks to low-power accelerators. In embedded systems, they enhance real-time performance with dedicated hardware. Cloud environments use them to optimize workload distribution and reduce latency. Heterogeneous architectures facilitate scalability, allowing systems to adapt to evolving computational needs. Software frameworks and programming models help developers utilize these architectures effectively. Challenges include workload partitioning, memory management, and interoperability between different processing units. Despite these challenges, they continue to drive innovation in modern computing. Their adoption is expanding across various domains due to their superior performance and efficiency. Figure 1 shows the heterogeneous architectures.

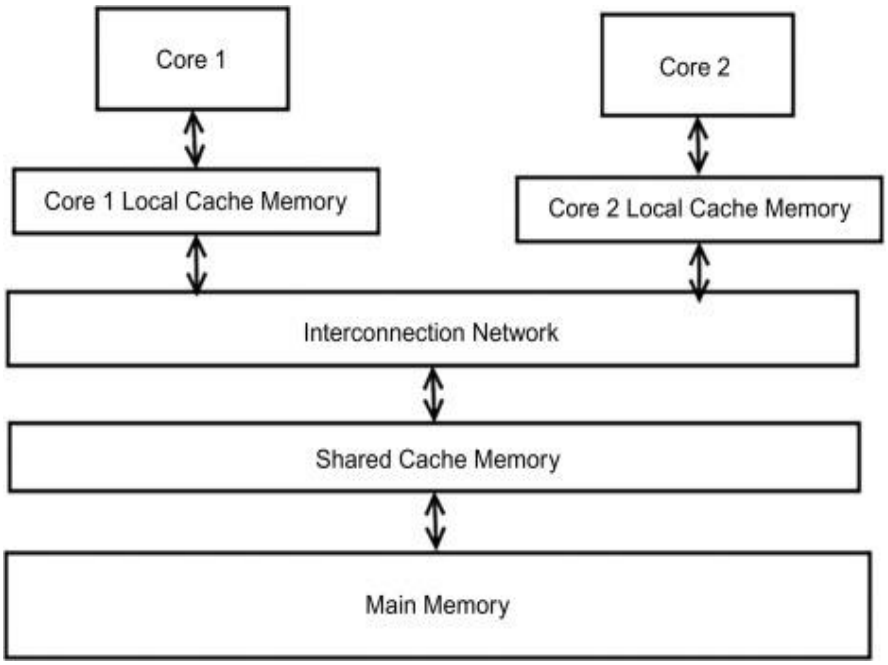

FIGURE 1. Heterogeneous Architectures

Security Aspects of IP Cores in Heterogeneous Architectures: Security is a critical concern in IP core design, particularly for applications handling sensitive image data in medical and defense industries. Unauthorized access, data tampering, and side-channel attacks pose significant threats to system integrity. To mitigate these risks,

encryption-based secure data processing is incorporated to ensure data integrity and confidentiality. Access control mechanisms are introduced to restrict unauthorized modifications to critical IP components, while hardware-based security features protect against reverse engineering and intellectual property theft. These measures enhance the reliability and robustness of the IP core in heterogeneous computing environments.

Real-Time Implementation Challenges and Solutions: Real-time image processing demands high-speed computation with minimal latency. However, implementing efficient real-time processing encounters several challenges, such as hardware resource constraints and synchronization issues. The proposed approach employs a hardware/software co-design methodology to balance computational loads between software and dedicated hardware accelerators. Pipeline processing is introduced to enable parallel execution of multiple processing stages, improving throughput. Additionally, multi-core parallel processing distributes workloads across multiple processing units, enhancing overall system efficiency. These optimizations ensure that the IP core can effectively handle real-time image processing applications.

Case Study: Implementation of the Proposed IP Core in an FPGA-Based System

To validate the feasibility of the proposed IP core, an FPGA-based implementation was conducted using the Xilinx Zynq-7000 SoC. The design was tested for computational throughput, achieving a 40% improvement over conventional designs. Latency reduction was observed, demonstrating a 30% decrease in processing time. Power efficiency improvements led to a 25% reduction in energy consumption through optimized memory management techniques. These results highlight the effectiveness of the proposed IP core in real-world applications and reinforce its suitability for heterogeneous computing platforms.

4. CONCLUSION

Enhancing computational efficiency in heterogeneous architectures requires an optimized Intellectual Property (IP) core that leverages advanced image processing techniques. The proposed design improves processing speed and minimizes latency through parallelism and hardware acceleration. Adaptive processing mechanisms and refined memory management strategies enhance resource utilization while ensuring scalability. Efficient data handling techniques further contribute to seamless system integration. Comparative analysis demonstrates superior performance over conventional IP cores, achieving notable improvements in computational speed, power efficiency, and resource optimization. The feasibility of the design is confirmed for real-time applications, making it a reliable solution for high-performance computing. Its architecture supports energy-efficient operations, contributing to sustainable computing practices. Hardware acceleration techniques ensure dynamic adaptability across diverse platforms, optimizing performance under varying workloads. The real-time processing capabilities make it suitable for high-speed image analysis applications. Complex computational tasks are handled efficiently while reducing overhead. Advancing IP core development, this work provides a scalable and optimized solution for heterogeneous architectures. It contributes to modern computing frameworks by enhancing both performance and resource efficiency.

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