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A Study and Design of Current Starved Ring Resonator On 16 nm Technologies

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Abstract
This research investigates distinct properties of Current Starved Ring Oscillator (CSRO) devices and proposes four novel layouts. A novel variable, called the Phase Noise Bandwidth Product (PNBP), is provided as well to solve the issue of choosing among phase disturbance effectiveness and wavelength adjusting capability when constructing Ring Oscillators (ROs). The suggested designs are evaluated against current designs with regard to of phase noise, electrical power utilization, frequency internet access, Power Delay Product (PDP). Three-stage CSROs were developed in Cadence technology to evaluate productivity employing the 16 nm PTM High Performance (HP) innovation framework. The simulation findings show that both of the independently suggested CSRO structures employing single NMOS sink and one PMOS supply achieve equivalent maximum outcomes in terms of PDP and PNBP to the conventional CSRO utilizing a result switching system, but with less surface need. Furthermore, when contrasted with standard CSRO, every one of the suggested designs outperform the latter in terms of both PNBP and PDP. The effectiveness of the CSROs is tracked as well with regard to fluctuations in Process-Voltage-Temperature (PVT) factors.
Keywords: PVT variations, CSRO, PNBP, current source, PDP, current sink**.**

Introduction

The Voltage-Controlled Oscillator (VCO) is a critical component of the Phase Lock Loop (PLL) for networked communications, generating clock signals and selecting frequencies [1]. In developing a VCO, it is critical to consider factors that include low power usage, broad intervals of procedure, and large absorption the ability [2,3]. A simple Single Ended Ring Oscillator (SERO) is made up of a plurality of amplifiers with degenerate load capacities at the output of each of them [4]. Every converter step provides a delay, therefore affects the duration of vibration. The total amount of electrical energy provided to power or drain each phase's capacitive burden influences dissemination delay [5]. The speed at which the VCO oscillates is directly related to the total amount of the charging (t_{ch}) and satisfying time (t_{dis}) [6] and is given by equation (1), where I_{bias} is the present throughout each step, N is the amount of phases, C_{tot} is the charge impedance of every phase, and VDD is the source.

$$f_{osc} = \frac{1}{N(t_{ch}+t_{dis})} = \frac{I_{bias}}{NC_{tot}V_{DD}} \quad (1)$$

Additional MOSFETs in series with the CMOS inverters can increase the equivalent resistance and limit the current flow. Such a circuit is known as a current starved ring oscillator (CSRO). SERO commonly employs the current starved (CS) delay phase for applications with little power [5]. While the CSRO consumes less energy, the lower current has a negative impact on the highest frequency, adjusting spectrum, and uniformity of the harmonic-voltage curve. The literature [7-9] describes many CSRO configurations that use various impacting devices. The delay step may be additionally modified to mitigate the disadvantages of the traditional CSRO. A CSRO is provided in [10], that employs an output-switch system. A CSRO utilizing just NMOS present drains and no bias device is shown in [11] to minimize the level of difficulty and influence usage. Jovanovic and Stojcev [12] proposed a delay feature with more predictability than the conventional layout.

The current investigation aims to investigate various CSRO designs in one technological setting and provide novel CSRO circuitry models. A novel efficiency metric, the PNBP, is provided as well to solve the phase-bandwidth compromise when evaluating oscillator designs. All of the devices are then evaluated in terms of energy use, frequencies connectivity, highest the rate, PDP and PNBP. Cadence Virtuoso system is used to simulate three-stage CSROs based on the 16 nm PTM HP technical model.

Existing CSRO Architectures

Conventional CSRO: Figure 1 depicts the simplest standard CSRO construction, consisting of NMOS current sinks (M13-M15), PMOS sources of electricity (M10-M12), an offset circuit (M1-M3), as well as straightforward CMOS integrators (M4-M9). The exterior control voltage, V_{ctrl}. regulates the orientation of the flow and, consequently, the frequency of the signal. The alternating current mirror technique is used to mirror the electrical voltage that is produced by the negative bias circuit onto the inverters in the circuit. Figure 1 depicts the most basic prevalent CSRO design, which contains a biasing circuit (M1-M3), NMOS present drains (M13-M15), basic CMOS converters (M4-M9) and PMOS sources of current (M10-M12). The outside control voltage V_{ctrl} , controls the bias current and thus the rate of change. The electrical current is produced by the bias circuit and mirrored onto the inverter components utilizing the current-generating reflection method.

To maintain uniformity over an extensive spectrum of frequencies, the bias current has to fluctuate proportionally alongside a variation of the controlling voltage. However, in a standard strategy for a specific band of regulation voltage, PMOS runs in the point of saturation whereas second (NMOS) behaves in the linear region, resulting in variability in the conditioning current. The working area of the Current Source Transistors (CSTs) also influences the consistency of the VCO. Because the switch potential is large, CSTs function in the triode area, and gateway inputs have fewer influence on bias present [13]. The end significance is a smaller spectrum adjustment region. In addition, the interlocking of M13-M15 elimination levels with the ultimate power of each step previous to load capacitance discharging increases the lag time.

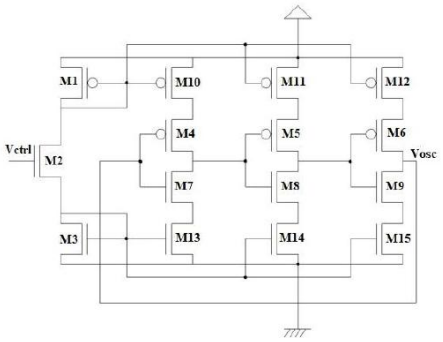

Figure 1. Conventional CSRO

CSRO with Production Switch System: In the CSRO design using the output-switch approach [10], the location of both of the controlling transistor in sequence alongside the CMOS converter differs from the standard CSRO, as shown in Figure 2. The CMOS integrators are made up of semiconductors M4-M9, while the CS components are M10-M15. At an increasing input, the generated impedance constantly drains from VDD, and quicker for the equivalent power controlled by semiconductors than in the typical circuit [8]. The discharge time varies irrespective of the imbalance between the inverting semiconductors. In comparison to the traditional system, the planning technique had minimal effect on variance in processes.

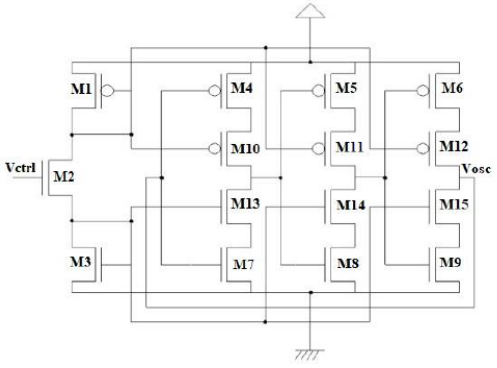

Figure 2. CSRO with output switch scheme

CSRO with solitary NMOS bowls: Dinesh and Bharadwaj [11] develop a CSRO utilizing just NMOS drains or remove PMOS inputs and reflection parts to minimize difficulty, die space, and energy use. Even the NMOS sinks retain authority over the state of affairs in all stages. The circuit demonstrated acceptable linearity and low phase noise characteristics. In order to regulate the duration, the V_{DD} rather than using a different control frequency. As illustrated in Figure 3, the bias circuit has been included with the NMOS sinks (M10-M12) for the sake of consistent comparison in this research. The oscillating frequency can be raised by increasing the current by removing PMOS sources, which lowers each circuit's overall impedance.

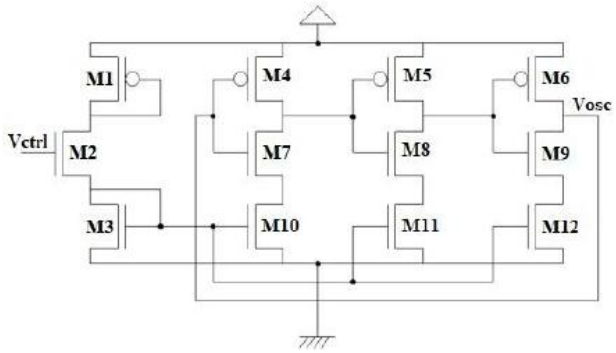

Figure 3. CSRO through NMOS present descends

RO through CS proportional masses: Several kinds of voltage control may not be appropriate for typical CS postponement units. The fluctuating delay line's effectiveness is harmed by the output propagation time fluctuation, which is not uniform with regard to the adjustment voltage. In order to assist in making the semiconductors M10-M21 work in maximum mode, a redesigned design is suggested [12] that adds transistors in series with CSTs as homogeneous loads. Because of this, the electrical charge that passes across MOSFETs is no longer influenced by the voltage coming from the source, improving the phase interference and maintaining stability against feed noise. Despite the expense of a smaller range, the use of symmetrical load enhanced predictability. In comparison to the conventional layout, the alteration leads to in higher discharge and charging current, which raises the speed of oscillation. Yet, more delay regulation is achieved when source semiconductor sizes are greater than drain emitter lengths. Figure 4 depicts a three-stage RO containing CS equal loads.

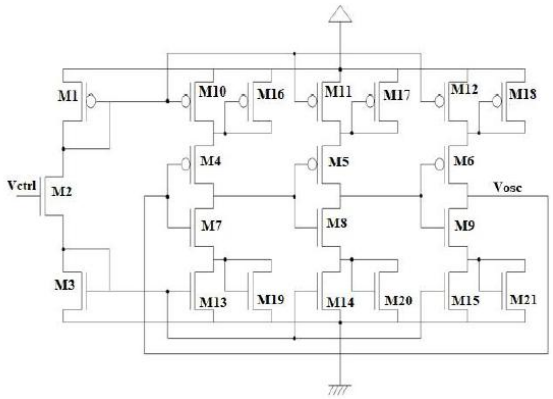

Figure 4. RO through CS balanced consignment junction transistor

Anticipated CSRO Designs

This work presents and examines 4 novel CSRO electrical circuits: 1 CSRO network containing only PMOS inputs (PO1), 1 NMOS outlet (PO2), 1 PMOS resource (PO3), and 1 supplier-sink combination (PO4). As seen in Figure 5(a), the initial circuitry is an alternative design to the circuitry in [11], in which semiconductors M10–M12 serve as the PMOS current generators and the NMOS current drains are removed from the standard network. In the final circuit arrangement, every stage's three distinct NMOS present sinks are combined into a single sink that has a triple width aspect. Figure 5(b) depicts the circuit using M10 as the lone NMOS decaying transistor. With an extra PMOS electrical source in place of the solitary present sink semiconductor, the third system offers an alternative to the preceding setup. The CSRO framework with a single PMOS current-generating semiconductor M10 is displayed in Figure 5(c). Both parasitic capacitance and the total amount of semiconductors needed are decreased by using a single NMOS or PMOS. It is anticipated that the reduced inductance will enhance

the delay thus improving the circuit's speed effectiveness. Single NMOS power sink and one PMOS basis of electricity for all three phases together make up the final suggested circuit. The only CS combination for each of the three divisions is composed of semiconductors M10 and M11 in Figure 5(d). At the expense of a reduced frequency range, the additional semiconductor in PO4 above PO2 and PO3 will increase the electrical influence that the course need.

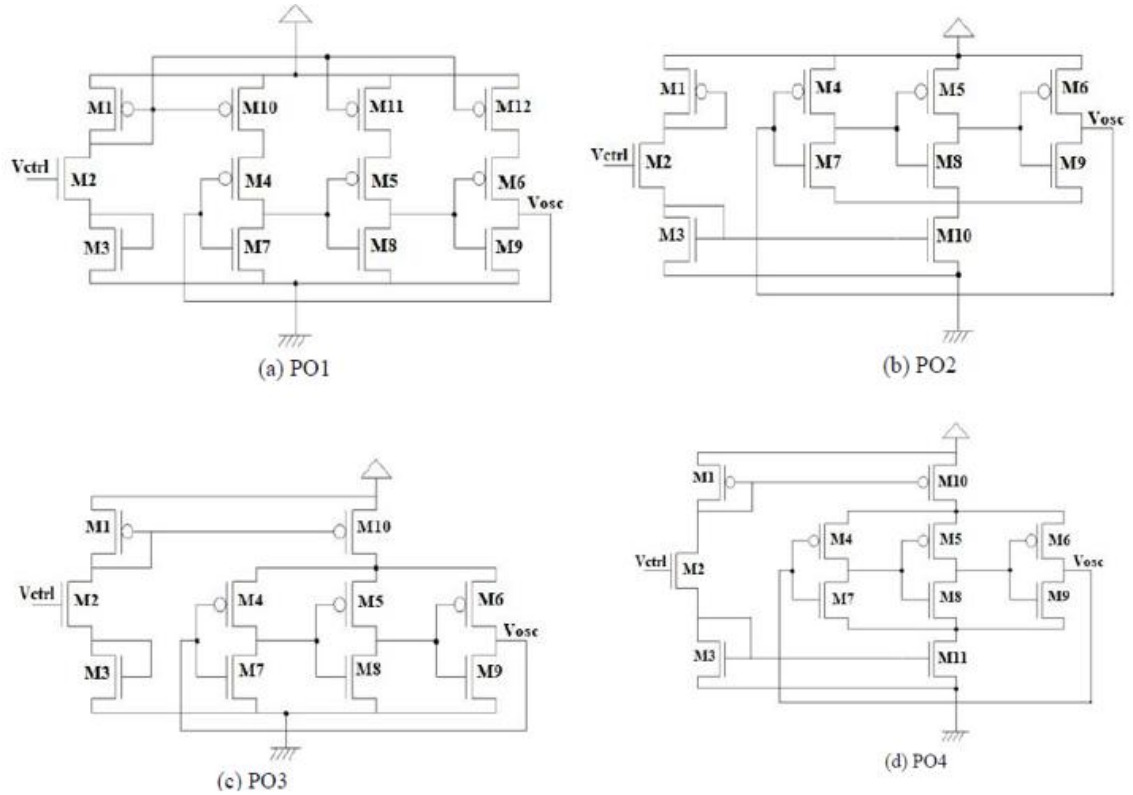

Figure 5. Proposed 4 dissimilar CSRO buildings

Results and Analysis

Simulation Environment: Utilizing the Cadence Virtuoso system, each of the current devices and 4 additional circuits have been replicated in 16 nm PTM-HP technology. Each of the eight circuits have the same influencing circuit layout for an equitable comparison. Table 1 lists the sizes of MOSFETs for the various circuit elements. Since the ideal size of the transistor for each of the many layouts is not examined in this work, they are not everyone uniformly ideal. For consistent comparison, that generates oscillation in the selected modeling settings, the same size is utilized. To achieve oscillation, the semiconductor transistor sizes for the CS and converter components are changed in the design in [10]. Additionally, the same amount of space is needed as with a traditional circuit. For frequencies tuning, the controlling supply V_{ctrl} is adjusted among 0.3 V and 1.0 V, whereas the power value V_{DD} is maintained at 0.5 V.

Table 1. Measurements of MOSFETs for Various CSRO Designs

Circuit	MOSFET Breadths (nm)		
	CMOS Inverter	CS Junction transistor	Bias Circuit
Conservative CSRO	W_n =320 W_p =640	W_n=32 W_p =64	W_n = 32 W_p=64
[12]		W_n=32 W_p =64	
[11]		W_n =96 W_p =192	
PO1		W_n=96 W_p =192	
PO2		W_n =320 W_p=640	
PO3			
PO4			
[10]	W_n = 32 W_p=64		

Power and Frequency Performance: Table 2 displays the devices' effectiveness according to multiple characteristics. The highest control voltage of 1 V is used to compute the power and frequency maximum

characteristics. Because there are fewer semiconductor devices in the suggested circuits PO1–PO3 than in the traditional circuit, the total comparable resistance is lower, which raises the electrical current. (1) states that a higher current will cause the circuit's operating speed rise (or its delay to decrease). Additionally, the CS devices from every stage are merged into an additional transistor in components PO2-PO4, which triples in diameter. The transistor's internal size (W and L), carrier flexibility (μ), oxide capacitor (C_{OX}), drain-source power (V_{DS}), gate-source voltage (V_{GS}), and threshold voltage (V_T) all affect the amount of current flowing through a MOSFET, as indicated by equation (2). Through influencing the threshold voltage, which has an inverse correlation with semiconductor size, the semiconductor transistor width also indirectly influences the current magnitude [14]. However, the three stages now share and split the single transistors' susceptibility in PO2-PO4, which ultimately lowers the overall problematic capacitor. Because of these events, the vacillating frequency of the suggested circuits is considerably higher than that of the typical circuit.

$$I_{bias} = \mu C_{OX} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right] \quad (2)$$

There is a compromise among speed and electricity when building a RO because a rise in current also results in an increase in the circuit's power usage. The findings in Table 2 additionally show that connection. In order to handle this issue of compromise and show which architecture yields the best outcome, it is crucial to compare the PDP effectiveness with several synthesizers. The circuit's delay of propagation and energy use combine to form the PDP. Since the oscillation frequency equals the inverse of the circuit's timing delay, the PDP is computed utilizing equation (3) at V_{ctrl} = 1 V and V_{DD} = 0.5 V. In brackets that are durable the measurements are indicated. The PDP efficiency for different architectures is shown in Table 2. A circuit that is quick and uses fewer watts should have a lower PDP value.

$$PDP(fJ) = \frac{power(nW)}{maximum\ frequency\ (MHz)} \quad (3)$$

Performance of Bandwidth and Phase-Noise: Table 2 also displays the relative phase noise efficiency and spectrum tweaking range of the various CSRO topologies. The controlling voltage is adjusted among 0.3 V and 1 V for the tunable region. For V_{ctrl} = 1 V, the period of noise is computed at an offset frequency equal to 1 MHz. A higher figure denotes greater distortion protection. For each phase disturbance absolute figures are provided; the true amount is minus.

The following examination of the tuning spectrum and phase noise values reveals the existence of an additional significant trade-off in ROs, namely that an oscillator's tuning band has a negative impact on noise efficiency. The total amount of phase noise falls as the temporal adjusting range expands. A new variable is suggested to handle this trade-off; it is computed using equation (4) and is the combination of the circuit's fundamental spectrum and unrestricted phase noise. A circuit with a large tuneable band along with acceptable phase instability efficiency should have a high PNBP rating. As a result, circuits with larger PNBP values offer superior compromise minimization. Consequently, whereas choosing or building the right RO circuit, this setting is just as crucial as the PDP.

$$PNBP(kdB) = \frac{phase\ noise\left(\frac{dB}{Hz}\right) \times tuning\ range(MHz)}{1000} \quad (4)$$

Table 2. Performance of Different CSRO Architectures

Building	Power(nW)	Maximum Frequency (MHz)	PDP (fJ)	Tuning Range (MHz)	Phase Noise @1Mhz(dBc/Hz)	PNBP (kdB)
Conventional	156.20	35.57	2.12	24.19	67.51	1.80
[10]	146.40	320.14	0.29	264.87	78.13	19.62
[11]	120.10	156.07	2.37	137.86	69.47	8.11
[12]	178.07	34.26	2.67	17.87	78.92	1.31
PO1	248.50	164.3	1.23	127.56	73.58	9.23
PO2	272.30	231.54	0.68	156.60	56.23	17.26
PO3	232.80	217.12	0.62	147.19	70.14	19.14
PO4	161.70	260.64	1.05	132.90	65.89	12.08

Response to PVT Variation: V_{DD}, V_T, and C_{OX} all affect the electrical current flowing across a semiconductor transistor. The relationship between the layer of oxide T_{OX} and the oxide capacitive C_{OX} is negative. VT and μ, on the other hand, rely upon the outside temperature. As a result, it is crucial to monitor how the oscillation frequency changes in accordance with supply, humidity, and process conditions. The oxide coating thickness of NMOS

transistors T_{OXN}, oxidation depth of transistors made of PMOS TOXP, and the voltage thresholds of NMOS diodes V_{TN} and V_{TP} have been considered to be process-related variables [15].

The ambient temperature, electricity voltage, and process variables are adjusted from -10% to +10% of their initial values. Table 3 displays the amount of frequency responsiveness in relation to the change. The tuning window is filled with frequency deviation, and the center harmonic is assessed utilizing the values that are ideal. The level of frequency fluctuation is computed using equation (5).

$$\%\ Frequency\ Variation = \frac{tuning\ range}{center\ frequency} \quad (5)$$

Table 3. PVT Variability' Impact on Changing Velocity

Parameter		**T**	**V_{DD}**	**V_{TN}**	**V_{TP}**	**T_{OXN}**	**T_{OXP}**
Idea values		27° C	0.5 V	0.48 V	-0.43 V	0.95 nm	1nm
Frequency Variation (%)	Conventional	0.90	135.3	132.7	106.2	57.08	41.28
	[10]	-1.47	112.5	93.1	85.8	46.59	45.05
	[11]	1.27	121.6	129.9	31.8	60.02	53.63
	[12]	1.33	119.8	104.6	110.2	60.03	53.31
	PO1	0.12	221.04	115.7	112.7	34.97	71.24
	PO2	0.86	113.79	132.6	25.6	87.47	31.23
	PO3	0.83	115.11	87.2	117.4	34.12	73.30
	PO4	1.67	123.22	137.6	118.2	71.60	46.13

Table 3's simulation findings demonstrate that every circuit is more sensitive to certain parameters than the others. Compared to the circuits in [10–12], the suggested circuits PO2 and PO3 exhibit superior stability in temperature. In terms of both supply and V_{TN}, the circuit in [10] exhibits the most stability, whereas in terms of V_{TP}, the circuit in [11] exhibits greatest instability. When compared to T_{OXP} and T_{OXN}, respectively, the suggested circuitry PO2 and PO3 exhibit the smallest amount of fluctuation in frequency.

Conclusion

The existing research contains a variety of CS delaying stage layouts, and this work examines the potential of four novel CSRO designs. Eight distinct circuits are evaluated overall based on important characteristics such power use, phasing noise, tuning range, and maximal velocity. The recognized PDP and the recently introduced PNBP are two significant features that can be utilized when comparing various synthesizers in order to take into account the differences between these parameters. According to research on simulation, the output switch approach in the current CSRO architecture offers the best PDP and PNBP efficiency. Nevertheless, the suggested CSRO designs PO3 and PO4 offer nearly identical PDP and PNBP performance with a significantly lower semiconductor count (5 fewer transistors), which results in a smaller space need. Despite having the largest and smallest power requirements and lowest phase noise values, respectively, these two novel circuit approaches offer very strong frequency effectiveness. When contrasted with the current CSRO approach with only NMOS absorbs, the suggested circuit PO1 offers a lower PDP value and a greater PNBP value, making it a superior substitute. RO provides very poor bandwidth and bandwidth efficiency, even though it offers superior phase noise efficiency and significantly decreased electrical consumption when used with CS asymmetric loads. In terms of PDP and PNBP, all four of the suggested topologies perform significantly better than the traditional CSRO circuit. The suggested circuit PO2 exhibits good stability in temperature, VTP, and T_{OXP} with regard to the fluctuations in PVT settings, while PO3 exhibits good consistency in humidity, V_{TN}, and T_{OXN}.

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