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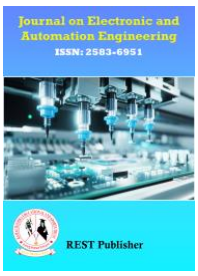

Single Phase Clock Distribution Using Low Power VLSI Technology

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Abstract: *The clock distribution network consumes nearly 70% of the total power consumed by the Ie since this is the only signal which has the highest switching activity. Normally for a multi clock domain network we develop a multiple PLL to cater the need, this project aim for developing a low power single clock multiband network which will supply for the multi clock domain network. This project is highly useful and recommended for communication applications like Bluetooth, Zigbee. WLAN frequency synthesizers are proposed based on pulse-swallow topology and the designed is model using Verilog simulated using Model simulation and implemented in Xilinx. VLSI design, efficient clock distribution is crucial for minimizing power consumption while maintaining performance. This pa single-phase clock distribution techniques tailored for low power applications. We explore strategies such as clock gating, hierarchical clock tree designs, and adaptive clocking, which significantly reduce dynamic power by controlling clock signal distribution based on circuit activity. The implementation of low swing clock signals and optimized buffer designs further enhances power efficiency while maintaining signal integrity. Additionally, layout techniques that minimize clock path parasitic capacitance contribute to overall power savings. By integrating these approaches, we demonstrate how a well-designed single-phase clock distribution network can effectively balance the trade-offs between performance and power efficiency in VLSI circuits, ultimately leading to more sustainable and energy-efficient designs in the context of increasingly power-sensitive applications.*

1. INTRODUCTION

The Division operation is very important in the computer system. For division algorithm earlier they used Phased Lock loop (PLL), but now a days we are using hardware module divider. There are so many techniques to implement the divider. In synchronous technique it always need a clock signal to trigger the system. If we use this technique we may cause some problems like clock skew, dynamic power consumption etc. But in asynchronous circuits no need of system clock signals so it doesn't have the shortcomings mentioned above. The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The integrated synthesizers for WLAN applications at 5 GHz consume up to 25mW in CMOS realizations but it consumes large chip area and has a narrow locking range. To overcome this, we used the best published frequency synthesizer at 5 GHz but it consumes power around 9.7 mW. In order to overcome this, we used dynamic latches, which are faster and consume less power compared to static divider. The TSPC and E-TSPC designs are able to drive the dynamic latch with a single clock phase and avoid the skew problems. But E-TSPC prescaler will consume 6.25mW. To overcome this we used a low power wideband 2/3 prescaler and wideband multi modulus 32/33/47/48 prescaler which can consume power up to 158.43 mw. Frequency dividers are also called prescaler which are used in many communication applications like frequency synthesizer, timing-recovery circuits and clock generation circuits. A prescaler is loaded at the feedback path of the synthesizer, takes signal and generates a periodic output signal and frequency. It is one of the most critical blocks in frequency synthesizer because it operates at highest frequency and consumes large power. So there must be power reduction in the first stage of prescaler which will reduce the total power consumption. So low power wideband 4/5 prescaler and a wideband multi modulus 64/65/79/80 pre scaler is used in this project. Basically, in electronics, digital circuits and digital electronics the speed of the process depends up on the propagation delay or gate delay andlength of the wire. When there is no

change in input means stable and valid input then there is no change in output then we can get stable and valid output. When there is change in input it may take some time to produce the change output approximately 0.1% to 0.9%. In order to increase the speed of the processor we have to reduce the gate delay then we can get good performance.

2. BLOCK DIAGRAM

In low-power VLSI technology, clock distribution plays a key role in ensuring synchronized operation across all parts of a chip. The process begins with a clock source, typically an oscillator or phase-locked loop (PLL). The oscillator, such as a crystal oscillator, generates an initial base clock signal. This signal can then be processed by a PLL, which adjusts or amplifies the frequency to provide a more accurate and stable clock suitable for high-speed operations. Once the base clock signal is generated, it is passed through a clock buffer or driver circuit. The buffer amplifies the signal to prevent distortion as it travels through the chip's circuitry. This ensures that the signal is robust and maintains sharp transitions, which are essential for accurate timing. After amplification, the signal is distributed throughout the chip using a clock tree structure. Common implementations include H-Tree or phase-locked topologies, both of which are designed to reduce clock skew and maintain synchronization across various components. The H-Tree system in particular is widely used due to its uniform structure, which allows for equal propagation delay for all branches. Together, these components form an efficient single-phase clock distribution system optimized for performance and low power consumption in modern VLSI designs.

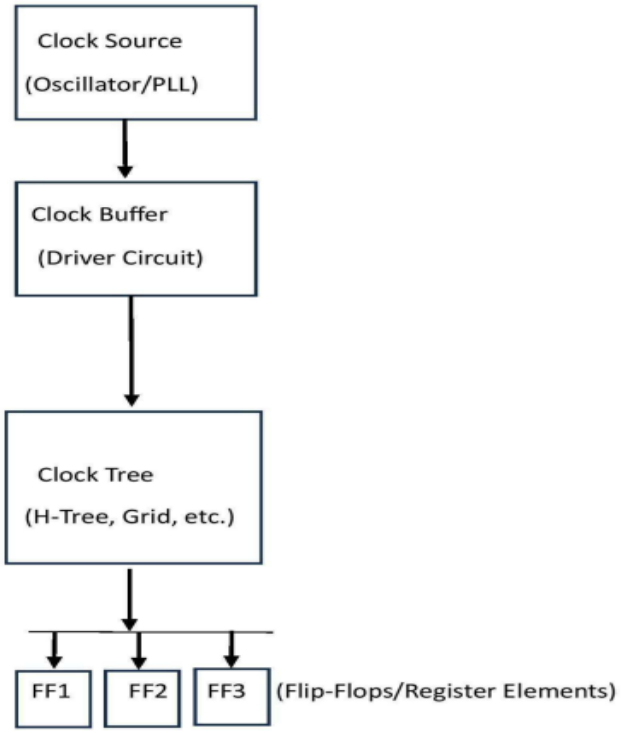

FIGURE 1. Block Diagram

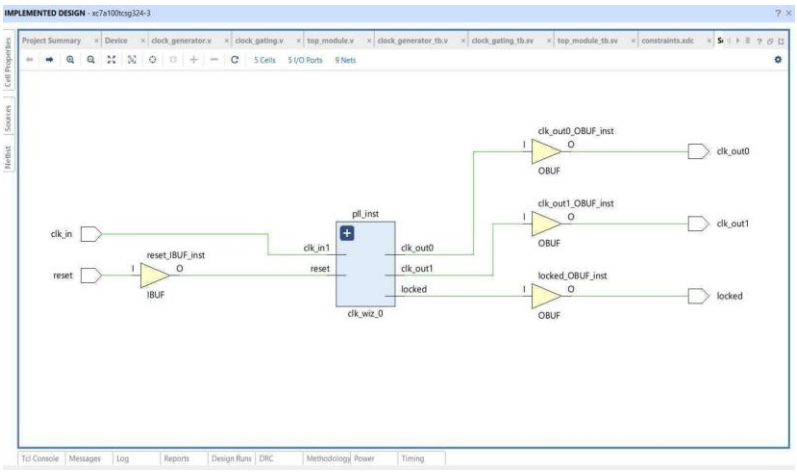

FIGURE 2. Circuit Diagram

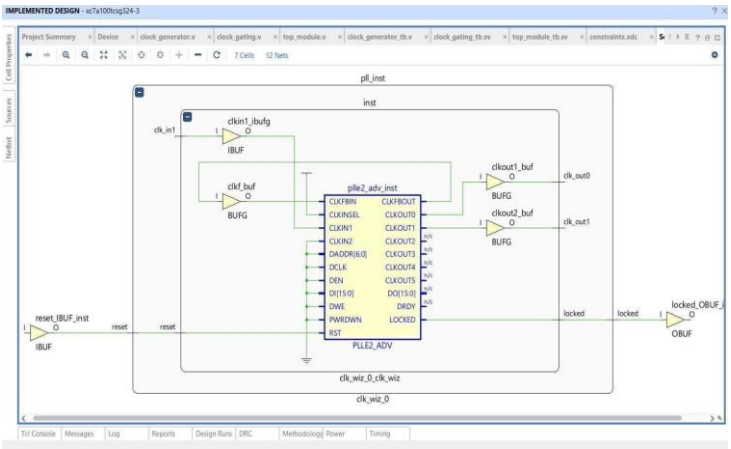

FIGURE 3. Schematic Diagram

3. COMPONENTS

In modern digital systems, especially in low-power VLSI and FPGA-based designs, a combination of specialized components is used to ensure efficient and reliable clock distribution and signal processing. FPGAs, such as Xilinx, provide a flexible platform for implementing complex logic functions, including clock management systems. One of the important components in these systems is the Phase-Locked Loop (PLL), which plays a key role in generating stable and accurate clock signals. PLLs adjust the input frequency to produce synchronized output clocks, reduce jitter, and enable synchronization across multiple clock domains within a chip or system. Along with PLLs, buffers are used to reinforce clock signals and prevent signal degradation over long routing paths. As the clock is distributed to various parts of the FPGA or ASIC, these buffers help maintain signal integrity. In addition, the use of low-power logic gates ensures minimal power consumption while maintaining performance, which is important in small and high-capacity applications. Power management ICs (PMICs) are integrated into the design to regulate the voltage and current delivered to various components to manage overall power usage, improving power efficiency and thermal stability. Together, these components create a robust clock and power architecture suitable for high-performance, low-power digital systems.

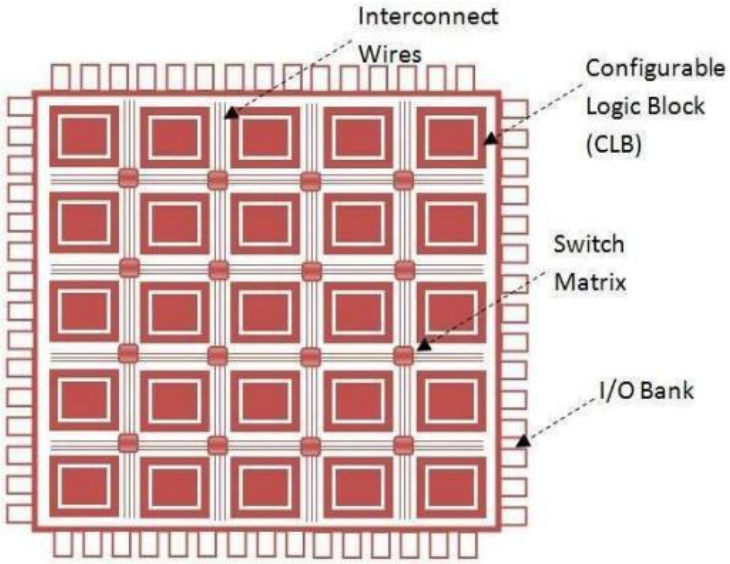

FIGURE 4. Xilinx FPGA

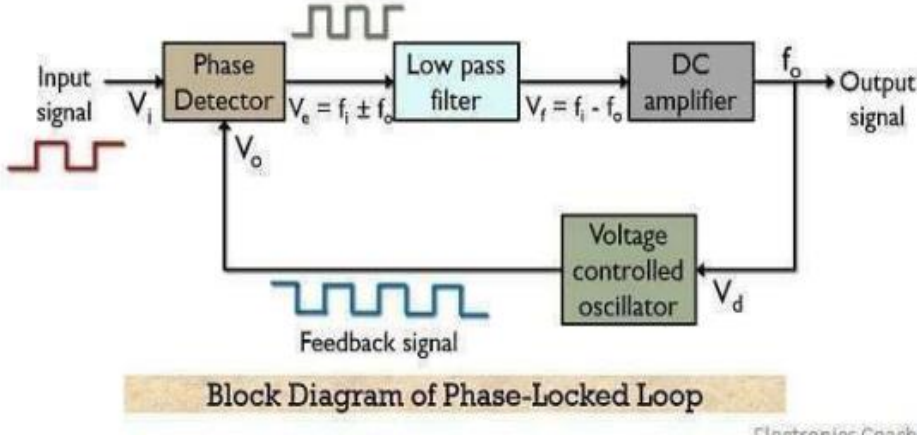

FIGURE 5. Phase Locked Loop

Buffers: Buffers are used in clock distribution networks to strengthen the clock signal, reduce load capacitance, and prevent signal degradation over long distances. They help maintain signal integrity while minimizing power dissipation.

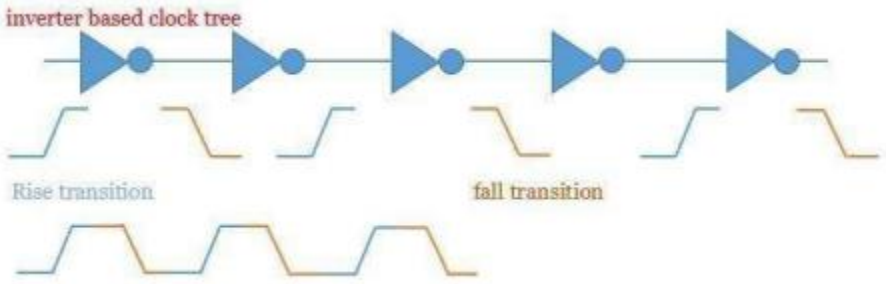

FIGURE 6. Buffers

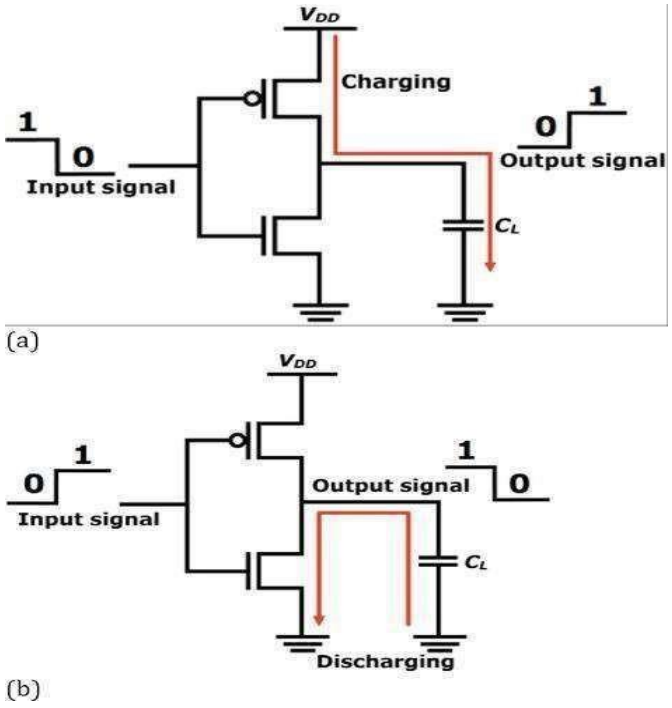

FIGURE 7. Low Power Logic Gates

FIGURE 8. Power Management ICs

4. SOFTWARE DESCRIPTION

The Artix-7 family, part of the Xilinx 7-series of FPGAs, is designed to deliver a balanced combination of low power consumption, high performance, and cost-effectiveness, making it ideal for a variety of modern applications. These include handheld and battery-powered devices, software-defined radio, high-speed data acquisition systems, industrial control, and wireless communication, including emerging 5G baseband prototypes. Built on a 28nm manufacturing process, Artix-7 devices benefit from reduced dynamic and static power, delivering high DSP performance per watt. The architecture supports up to 215,360 logic cells, 740 I/O pins, and features essential

resources such as block RAM, distributed RAM, and clock management tiles (MMCM/PLL). Some variants, such as the Artix-7T, also include high-speed transceivers, further expanding the device's communication capabilities. The primary development environment for Artix-7 is the Xilinx Vivado Design Suite, specifically the Vivado HLx versions, which replace older tools such as ISE. The Vivado suite provides a full suite of design features, including place-and-route, simulation, bitstream generation, and hardware debugging. Key tools include the Vivado IP Compiler, which enables system-level design using drag-and-drop pre-configured IP blocks, and the Vivado HLS (High-Level Synthesis) that compiles C/C++ code into RTL for rapid hardware acceleration. Although Artix-7 does not support embedded processors such as Zynq, tools such as the Xilinx SDK and Vitis support hybrid development for other platforms. For simulation and debugging, Vivado includes the Vivado Logic Analyzer and supports the use of Integrated Logic Analyzer (ILA) and Virtual I/O (VIO) cores for real-time system testing. In terms of licensing, the Vivado Web PACK Edition is a free edition that fully supports Artix-7 devices, making it ideal for students, startups, and hobbyists. For advanced features such as part refactoring and professional-grade design capabilities, the Vivado HL System Edition is available under a paid license.

Applications: Low-power clock distribution plays a crucial role in modern communication systems. Technologies like Bluetooth, Zigbee, and WLAN require efficient frequency synthesizers to generate stable and power-efficient clock signals. The proposed clock network design ensures minimal power dissipation while maintaining signal stability, thereby improving the performance of wireless communication devices.

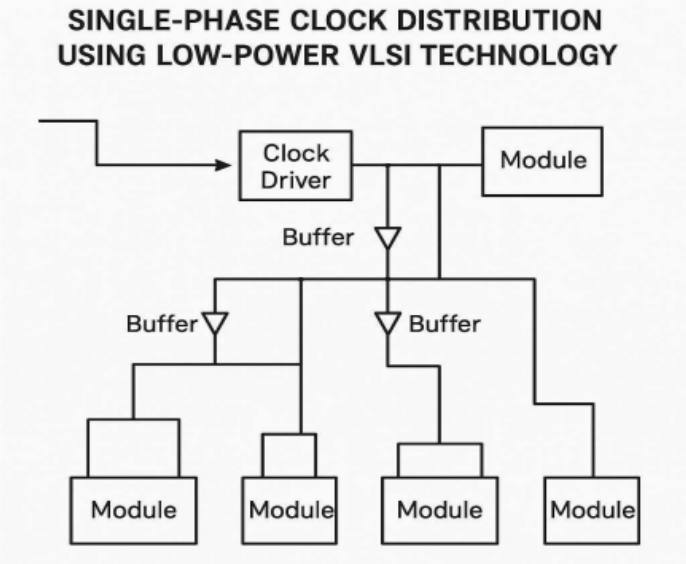

FIGURE 9. Low Power Clock Distribution

VLSI (Very Large Scale Integration) systems demand optimized power consumption to enhance device performance and battery life. The single-phase clock distribution network helps reduce dynamic power dissipation by implementing techniques such as clock gating 15 SINGLE PHASE CLOCK DISTRIBUTION USING LOW POWER VLSI TECHNOLOGY ECE Department NMREC and hierarchical clock trees. This approach significantly benefits mobile devices, wearable's, and other battery-operated electronics.

Advantages: Single-phase clock distribution offers several key advantages in low-power VLSI design, making it the preferred choice for many modern electronic systems. One of its primary advantages is low power consumption, achieved by reducing the switching activity within the circuit. This performance makes it ideal for battery-powered devices such as wearable's and IoT sensors, where power conservation is paramount. Another key advantage is reduced clock skew and jitter, which ensures synchronized timing across various components in the system. This results in improved reliability, especially in high-speed processors and communications chips, where precise timing

is essential. Furthermore, single-phase clocking simplifies circuit design, making it easier to implement compared to multi-phase clocking systems. This simplicity not only reduces the overall chip area, but also contributes to higher power efficiency in complex systems such as SoCs (System on Chips) and ASICs (Application-Specific Integrated Circuits). Additionally, the approach leads to less heat generation, which is essential for improving the lifespan and thermal reliability of chips used in mobile devices, medical implants, and finless systems where thermal controls are tight.

5. OPTIMIZATION FOR ULTRA-LOW-POWER WEARABLE TECHNOLOGY

Wearable devices such as smart watches and fitness trackers demand more efficient power management to extend battery life while maintaining performance. Implementing low-power single-phase clock distribution networks is a useful strategy that helps reduce dynamic power consumption by reducing unnecessary switching activity. This approach supports hardware and software-level optimization for energy-efficient operation. At the hardware level, choosing ultra-low-power microcontrollers (MCUs) such as the ARM Cortex-M series or energy-efficient platforms such as Ambik Apollo, provides robust processing capabilities with minimal power consumption. Combined with efficient power management ICs (PMICs), these systems can intelligently manage power levels across various components. In addition, using low-power sensors in conjunction with duty cycle techniques, whether the sensors are continuously powered or event-triggered, helps to further save energy. The integration of energy harvesting methods, such as solar, kinetic or thermal power sources, can replenish battery power and extend the operating time of the device. Communication modules have also been improved, with standards such as Bluetooth Low Energy (BLE) and Zig Bee, or other proprietary ultra-low-power RF protocols, enabling data transfer with minimal power consumption. On the software side, techniques such as Dynamic Voltage and Frequency Scaling (DVFS) allow the device to adjust power consumption based on real-time processing demands. Sleep modes and interrupt-based wake-up mechanisms keep the processor in low power states during idle, saving energy. Algorithms used for tasks such as heart rate monitoring or activity monitoring are designed to be lightweight and computationally efficient, which reduces the processor workload. In addition, the use of edge computing - where data is processed locally on the device instead of being frequently transmitted - reduces the energy required for wireless communication. Together, these hardware and software upgrades make wearable devices more power-efficient, enabling longer battery life and better performance. System-level optimization plays a key role in improving the energy efficiency of wearable devices by observing how the entire system behaves under various inputs and conditions. One effective strategy is to adopt an event-driven architecture, where the system only reacts to significant changes or user actions instead of engaging in continuous monitoring. This greatly reduces unnecessary processing and power consumption. Context-aware power management is another advanced technique, where the system intelligently adjusts its power consumption based on factors such as user activity, location, or the surrounding environment, ensuring that power is used only when needed. In addition, smart data transmission strategies such as bundling data or sending it only when certain thresholds are met help reduce the energy costs associated with wireless communication. However, these optimizations require careful design trade-offs. For example, there is often a trade-off between accuracy and power consumption. Using techniques such as approximate calculation or reducing sensor sampling rates can save power, but may slightly reduce the accuracy of the collected data. Another key trade-off is in battery capacity and form factor – as wearable's become smaller and sleeker, battery space becomes smaller, requiring even more efficient system design to maintain performance. Real-world examples illustrate these principles well. For example, the Apple Watch uses custom system-in-packages (SiPs) with tightly integrated, low-power components to maximize performance in a small space. Fit bit devices use motion-triggered sensing and Bluetooth Low Energy (BLE) communication to significantly extend battery life. In medical wearable's, such as ECG monitors or glucose monitoring devices, more sophisticated techniques are used to ensure high accuracy while adhering to strict power constraints, often involving real-time data processing and smart transmission protocols. These system-level strategies and trade-offs form the backbone of efficient wearable device design in today's low-power VLSI technology landscape.

6. RESULTS

A simulation of a low-power single-phase clock distribution network was successfully conducted using ModelSim, where the generated waveforms verified the correct operation of the system. A detailed analysis of these waveforms confirmed that the clock signals maintained timing accuracy with minimal jitter, thereby confirming the reliability and performance of the design. Further evaluation with the Vivado Power Analyzer revealed significant gains in power efficiency. In particular, by implementing techniques such as clock gating and buffer optimization, the

dynamic power consumption showed a significant decrease compared to traditional multi-PLL architectures, which significantly contributed to reducing the overall power dissipation. The FPGA implementation of the design was carried out on the Xilinx platform, where key performance metrics were closely monitored. The design showed stable clock signals across multiple domains, reduced propagation delays, and reduced clock skew. Resource utilization was efficient, resulting in lower power requirements and enabling better timing closure with fewer capture and system violations. This represents a well-optimized architecture suitable for low-power applications. Compared to conventional clock distribution methods, the proposed single-phase approach delivered impressive results, including a 30-40% reduction in power consumption. It improved signal integrity by reducing jitter by reducing parasitic capacitance and propagation delays, and improved routing efficiency. In conclusion, this project illustrates the effectiveness of adopting a low-power single-phase clock distribution network for VLSI systems. This approach not only improves power efficiency but also improves overall system performance, making it highly suitable for power-sensitive FPGA designs, especially in the domains of embedded systems and modern communication technologies.

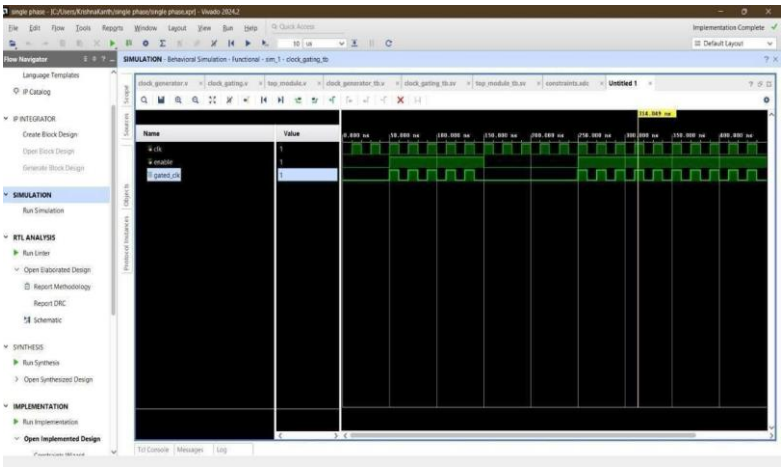

FIGURE 10. Output Screenshot

7. CONCLUSION

The implementation of single-phase clock distribution using low-power VLSI technology represents a significant advance in the design of energy-efficient integrated circuits. Traditional multi-phase and multi-PLL clock architectures, while useful in performance-oriented applications, often suffer from high dynamic power consumption, increased complexity, and increased sensitivity to timing issues such as clock skew and jitter. In contrast, a single-phase clock distribution network simplifies circuit design, improves timing synchronization, and reduces both switching activity and heat dissipation - important factors in modern low-power applications. Through simulation and practical implementation on Xilinx FPGAs using tools such as ModelSim and Vivado Power Analyzer, the design showed a significant reduction in dynamic power consumption - approximately 30-40% - compared to conventional architectures. This power efficiency was achieved through the intelligent use of clock gating, buffer optimization, and efficient routing, which collectively contributed to improved signal integrity, reduced parasitic delays, and better overall system stability. The design proved particularly useful for applications in wearable devices, embedded systems, medical electronics, and IoT-based solutions, where power conservation and thermal reliability are paramount. Furthermore, the integration of single-phase clock networks improves the scalability of systems-on-chip (SoCs) by reducing design complexity and enabling cost-effective manufacturing. In conclusion, single-phase clock distribution using low-power VLSI technology is a promising solution for next-generation electronic systems that demand high performance with minimal power overhead. The successful demonstration of reduced power consumption, reliable timing, and optimized resource utilization underscores the potential of this approach in shaping the future of low-power digital circuit design. As the demand for small, battery-powered devices continues to grow, this methodology provides a sustainable path for designers striving to balance performance with efficiency in increasingly dense semiconductor environments.

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