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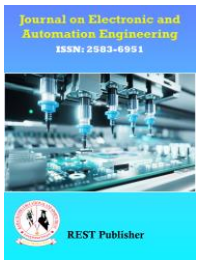

Radiation-Hardened 14T SRAM Cell Design for Double Node Upset Immunity in Space Applications

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Abstract: *Deep sub-micron memory technologies are essential parts of space-based electronics because of their vulnerability to Both double-end upsets (DNUs) and single-event upsets (SEUs). High-energy charged particles propagating through space can temporarily affect memory elements by disrupting the charge accumulated at critical nodes. A sturdy radiation-hardened-design (RHBD) SEI-14T SRAM cell, created especially for satellite and space systems, is presented in this work. The SEI-14T's dual-junction circuit layout lowers SEUs and DNUs across all sensing nodes with a self-correcting, state-reset feedback mechanism. Additionally, by maximizing the spatial spacing of the sensing zones, the design improves recovery from residual upset pairs. The performance advantages of the SEI-14T are illustrated by comparison with various state-of-the-art radiation-hardened memory cells, including the Quatro-10T, RHM-12T, RHD-12T, RSP-14T, RHPD-12T, RH-14T, EDP-12T, and QCCS-12T. The SEI-14T stands out with its remarkable read and write stability. At a supply voltage of 0.8V, the SEI-14T outperforms current designs by reducing steady-state power consumption by 20.82%, read access time by 23%, and write access time by 12.28%. In addition, the critical charge of the SEI-14T is significantly higher than that of alternative memory cells, with values that are 8.85, 6.56, 3.4, 5.75, 2.54, 2.47, 1.81, 1.63, and 1.44 times higher than those of 6T-SRAM, Quatro-10T, RHM-12T, RHD-12T, RSP-14T, RHPD-12T, RH-14T, EDP-12T, and QCCS-12T, respectively.*

Index terms: *soft faults, radiation hardening, sensitive tip, double-tip upset (DNU), ion track, PVT analysis, critical charge, and single-event upset (SEU).*

1. INTRODUCTION

Radiation-induced disturbances, particularly SEUs and DNUs, are one of the most significant challenges in space applications. These disturbances occur when high-energy particles strike a memory cell, causing changes in the stored data. In SRAM cells, this can result in a bit-flip, where a stored “1” changes to a “0” or vice versa, leading to incorrect data storage and potential system failures.

- Single-event upset (SEU): SEU refers to the flipping of a recorded data bit by a high-energy particle striking a sensitive node in a memory cell. If the system has error-correcting routines, this may cause a transient error that can be corrected.
- Double-Ended Upset (DNU): A DNU is more severe than an SEU because it involves the disturbance of two or more storage nodes simultaneously, leading to more significant errors in the memory. This makes DNUs harder to recover from, requiring more advanced error recovery mechanisms.

Numerous space agencies involved in space exploration have developed artificial satellites and spacecraft containing hundreds of electronic circuits and components. However, radiation, often Called "space radiation", it consists of high-energy particles and electromagnetic waves that penetrate the space outside the Earth's atmosphere. The stability and reliability of electronic systems are severely threatened by this radiation. Even the low-energy alpha particle can disrupt the normal functioning of electrical devices [1]. Over the past few decades, single-event effects (SEEs) have become a major cause of soft faults. The ongoing reduction in device geometry has notably increased the vulnerability

of integrated circuits to radiation-induced disruptions [2]. Space-based memory systems must operate in a highly dynamic environment, where radiation, temperature fluctuations, and other external factors can affect their performance. Traditional memory cells, such as 6-transistor (6T) The straightforward design of SRAM cells, which rely on cross-coupled inverters for data storage, makes them highly vulnerable to SEUs and DNUs. As device geometries shrink and the operating voltage is reduced, the critical charge (the amount of charge needed to flip a bit) decreases, making the memory cells more vulnerable to radiation-induced disturbances.

The main challenges faced by memory cells in space applications include:

- Susceptibility to Radiation: Memory cells in space must be designed to resist radiation-induced upsets and maintain data integrity.
- Stability Under Extreme Conditions: Memory cells must operate reliably under various conditions, including fluctuations in temperature, voltage, and process variations.
- Power Consumption: In space applications, minimizing power consumption is essential to ensure the longevity of the system. Radiation-hardened designs must balance power efficiency with robustness.

The SEI-14T SRAM cell is designed to mitigate the effects of radiation-induced disturbances, particularly SEUs and DNUs. It incorporates several advanced features to enhance its resilience and improve its stability under different environmental conditions.

Dual-Junction Architecture: The SEI-14T SRAM cell uses a dual-junction architecture, which includes two separate feedback loops. This structure reduces the memory cell's vulnerability to soft faults and improves its stability. SEI-14T is highly resistant to both SEUs and DNUs because it has two feedback loops that allow it to correct any disturbances in one of the other node storage nodes.

Self-Correcting Mechanism: The SEI-14T design includes a self-correcting mechanism that allows the memory cell to recover from soft errors caused by radiation. This mechanism ensures that even if one of the storage nodes is upset, the cell can recover and restore the correct data state.

State-Reset Feedback: The SEI-14T SRAM cell features a state-reset feedback mechanism that improves error correction capabilities. This feature ensures that any error introduced by radiation is quickly corrected, maintaining the integrity of the stored data.

Critical Charge Enhancement: The SEI-14T design maintains a higher critical charge than traditional SRAM cells, making it more resistant to radiation-induced disturbances. This is achieved by optimizing the transistor sizes and the layout of the memory cell to increase the charge required to flip a bit.

Improved Write and Read Stability: The SEI-14T SRAM cell offers enhanced write and read stability compared to traditional designs. This is particularly important in space applications, where fluctuations in temperature, voltage, and process variations can affect the performance of the memory cell.

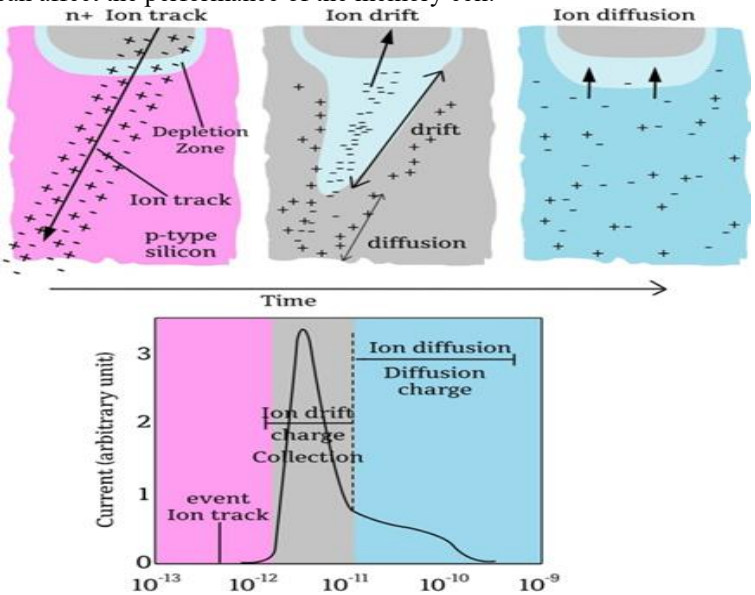

FIGURE 1. High-energy particle impact, ion footprint, and transient pulse generation.

2. RECENT ADVANCES IN RELIABLE RHBD SRAM MEMORY CELLS

The design of a standard 6-transistor (6T) SRAM cell uses a cross-coupled positive feedback loop. A bit-flip can happen, converting a stored "1" to a "0" if a high-energy radiation particle strikes one of the cell's sensitive ends and the charge it introduces beyond the critical threshold [7]. Standard SRAM is extremely susceptible to soft faults due to its cross-coupled architecture, which allows the disturbance to spread to the cell's other end. It is confirmed by experimental studies from [13] and [14] that normal SRAM cells are susceptible to disruptions caused by radiation. A number of radiation-hardened memory cell designs, to solve this problem, devices were developed, including the Quattro-10T, RHM-12T, RHD-12T, RSP-14T, RHPD-12T, RH-14T, EDP-12T, and QCCS-12T.

A. Quatro-10T

The Quatro-10T design incorporates a negative feedback recovery latch into the standard SRAM architecture to restore data lost due to radiation incidents., as illustrated in Figure 2(a). Its exceptional read stability during process, voltage, and temperature (PVT) fluctuations is one of its main advantages [15]. Its smaller critical charge than previous hardened designs, however, is a significant drawback because it prevents data recovery when the logic is set to "0."

B. RHM-12T

The RHM-12T design, depicted in Figure 2(b), features a pair of stacked PMOS transistors, enhancing the Quatro-10T design. As noted in [16], the PMOS stacking helps reduce read access time and steady-state power consumption. Despite these benefits, the design suffers from a reduced critical charge at low supply voltages and high write access latency, particularly at extreme temperatures (-45°C to 120°C).

C. RHD-12T

Figure 2(c) shows the RHD-12T, which is an improvement on the Quadro-10T system. Its most notable feature is its efficient error recovery mechanism [17]. However, the design struggles with a small critical charge at low supply voltages and exhibits slow write access during PVT fluctuations.

D. RSP-14T

The RSP-14T design, seen in Figure 2(d), builds on the RHD-12T by adding two additional transistors (P7 and P8). This enhances write performance at low supply voltages [18]. However, it only repairs damaged bits when the logic state is "1," and the shared charge between sense node pairs increases the likelihood of failure.

E. RHPD-12T

Figure 2(e) shows the RHPD-12T design, which increases write capacity by adding two more access transistors (N9 and N10). Compared to previous designs, it offers notable advantages such as a higher critical charge and improved read stability [19]. However, write access time remains an issue under PVT fluctuations.

F. RH-14T

To further improve the structure, the RH-14T SRAM cell uses stacked PMOS transistors (P1 and P2), as seen in Figure 2(f). By incorporating Including a pair of inverters (P7 and N5) in the design., this structure enables the creation of five distinct storage nodes. One of its key strengths is the ability to perform write operations and maintain data integrity even under severe PVT conditions [20]. Additionally, it boasts a higher critical charge compared to current memory cell designs. However, the main limitation is the high soft error failure rate caused by charge sharing between pairs of sensing nodes.

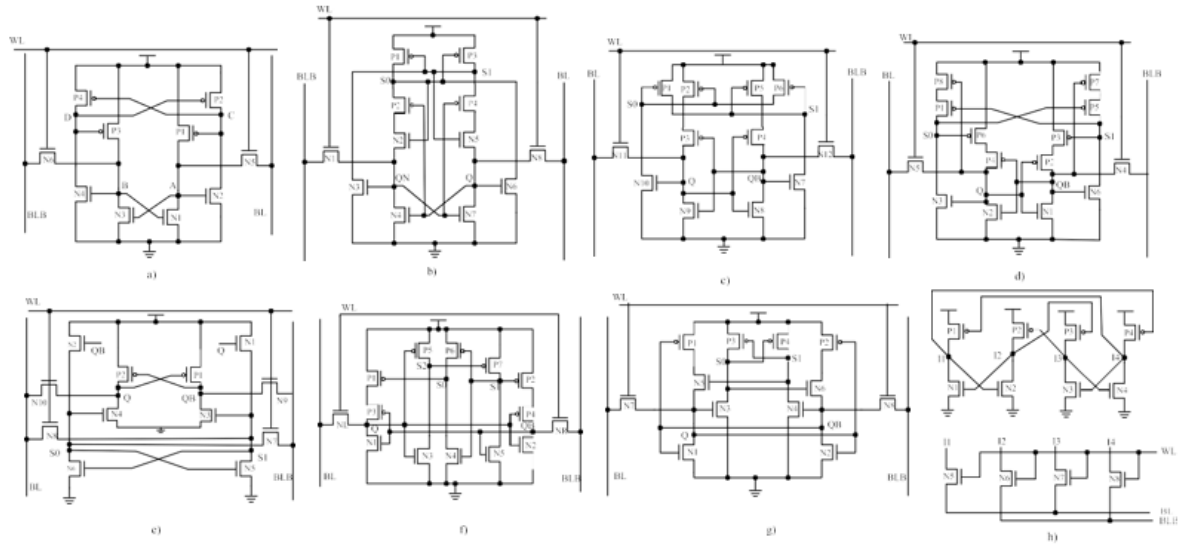

FIGURE 2. RHBD literature designs (Figure 2) are RHM-12Tc, RHD-12Td, RSP-14Te, RHPD-12Tf, RH-14Tg, EDP-12Th, QCCS-12T, and Quattro-10Tb.

G. EDP-12T

The EDP-12T cell, shown in Figure 2(g), adds transistors N5 and N6 to the RSP-14T structure. Its primary advantage lies in achieving fast write access times under varying PVT conditions [21]. However, when exposed to extreme temperatures and corner conditions, it suffers from poor read and write stability.

H. QCCS-12T

The QCCS-12T design improves upon DICE stands for Dual Interleaved Storage Cell [22]. As seen in Figure 2(h), it consists of four pairs of cross-coupled inverters. One of its advantages is that, unlike many hard memory cells, it has a high critical charge. and faster access times during PVT variations [23], [24]. However, due to shared sensitive nodes, it is prone to soft error recovery failures at a charge threshold of 70 fC.

3. ANALYSIS OF SOFT ERROR RECOVERY AND SEI-14T MEMORY CELL PERFORMANCE

To overcome the aforementioned limitations, the SEI-14T is introduced as a robust, soft error-resistant Memory cell with radiation-hardened design (RHBD) comprising 14 transistors. Some of its key technical benefits are:

- Outstanding stability: The SEI-14T maintains excellent read and write stability, even under extreme PVT fluctuations.
- Efficient operation: The cell features fast write access times and stable power consumption during PVT variations.
- High charge retention: It achieves high reliability by maintaining a significant charge in fluctuating supply voltages and corner cases.
- Soft error immunity: All sensitive nodes in the SEI-14T are fully protected from soft errors.
- Double-ended upset tolerance: The design can withstand double-ended upsets, thanks to the sensitive area separation technique.

The SEI-14T memory cell's layout and design are depicted in Figures 3 and 4. As shown in Figure 3, the structure incorporates improve write performance. Robust mistake correction is also guaranteed via a state-recovery feedback method that makes use of two latch circuits. are set up to lower the read current. Data communication with the storage nodes is made possible via bit lines that are coupled to the access transistors. Read and write operations are carried

out accompanying secondary node to return to its original logic state, and vice versa. Nodes QB and S0 store a "0," but nodes Q and S1 hold a logic "1." The basic functioning and error-correction behavior are assessed using this logic.

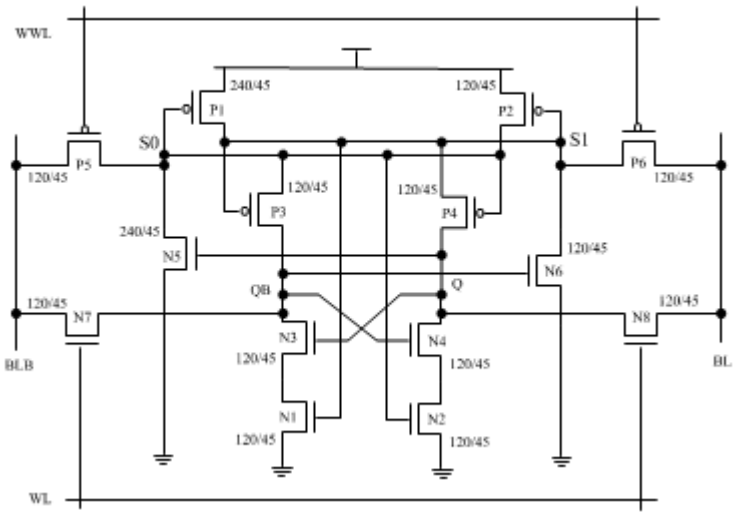

FIGURE 3. SEI-14T memory cell schematic diagram.

Stability:

Another essential component of memory cell performance is stability. Stability and soft error sensitivity are traded off in many memory cell designs covered in the literature. Therefore, it is of utmost importance to properly assess memory cell stability. Important indicators of memory cell stability are read, write, and hold performance. determine a memory cell's Read Static Noise Margin (RSNM) [7]. The capacitances driving the logic state affect the cell ratio (CR) and RSNM at the storage nodes [35]. We use a comparable cell ratio of two to assess all memory cells for a precise comparison. Figure 11 displays each radiation-hardened memory cell's RSNM values.

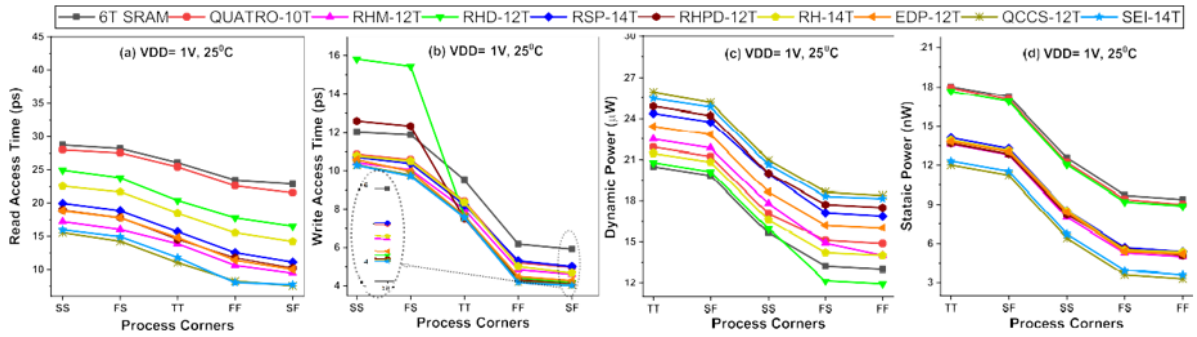

FIGURE 4. Results for read, write access time, dynamic power and static power for all designated memory cells at At 25◦C and 1V at various process angles (a) RAT at various angles (b) WAT at various angles b) Average dynamic power consumption for read and write at various angles d) Average static power dissipation at various angles.

Due to limited design tolerances for space and satellite applications, we have considered worst-case process corners (FS, SF, and FF) and temperatures (125°C and -45°C) for all memory cell types [34]. Figure 12 shows the contents of each memory cell. static noise margin (SNM) values under these harsh circumstances. The SEI-14T and RH-14T memory cells' poor logic drives at both primary storage nodes Q cause low read stability in all of the cells. The write steady-state noise margin (WSNM) is the ability of a memory cell to flip its recorded data during a write operation. According to [37], a useful method for estimating the write margin of a memory cell is the word line write travel voltage. To determine the write margin, the bit lines containing the data to be written are first set, the word line (WL)

voltage is raised to VDD, and the potential difference between VDD and WL is checked as it travels through the Q and QB nodes.

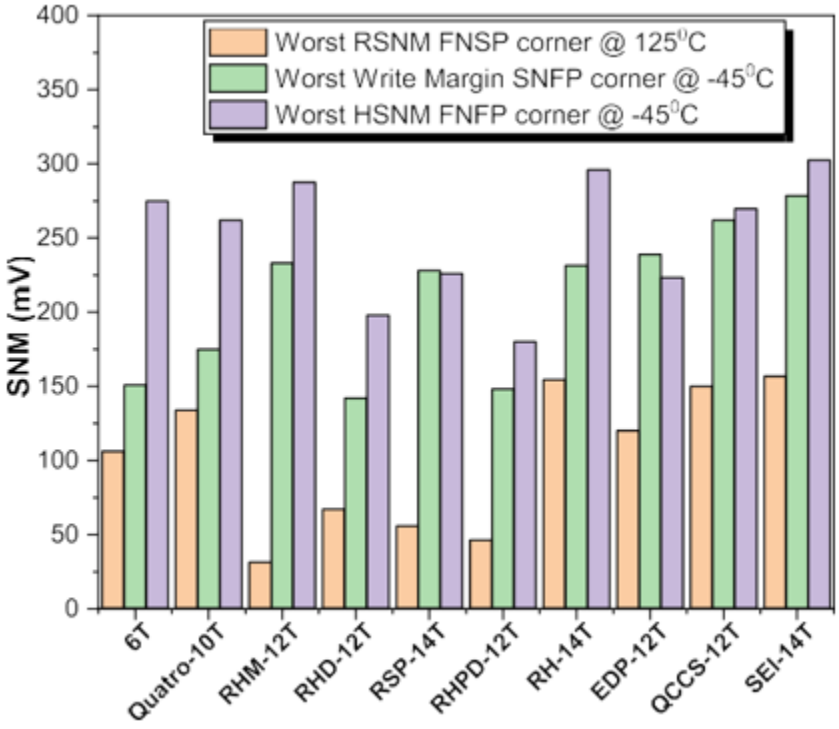

FIGURE 5. Comparison of stability and temperature analysis of all memory cells in the worst case.

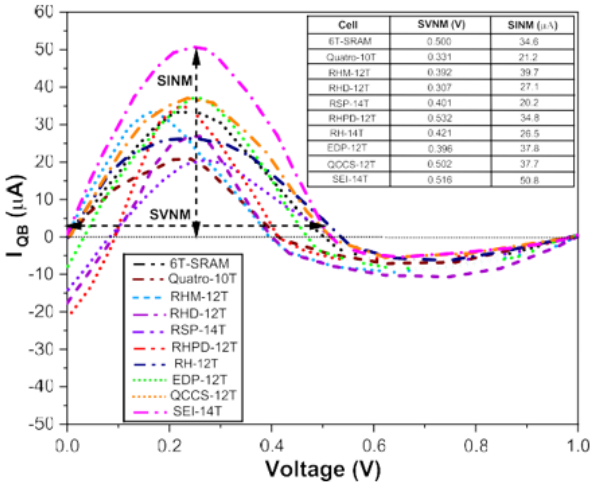

FIGURE 6. N-curve comparison of existing and proposed memory cells.

The N-curve method is used to evaluate the read stability of a memory cell. To confirm the read mode state of a memory cell, a voltage source is connected to the primary storage node "0". The current from the external voltage source, which shows the voltage and current characteristics during read. operation, is also taken into account [37]. Figure 13 compares the N-curve waveforms for each radiation-hardened memory cell. Every curve has three places of intersection with the x-axis The curve's amplitude defines the steady-state current noise margin (SINM), and The steady-state voltage noise margin (SVNM) is shown in the first two points. Among all the memory cells, RHPD-12

has the lowest RSNM and the largest SVNM. On the other hand, the SEI-14T memory cell exhibits the highest SVNM and SINM, indicating improved read stability, as higher SVNM and SINM values indicate improved stability.

To evaluate the performance of the SEI-14T SRAM cell, several metrics are considered, including read access time, write access time, critical charge, static and dynamic power consumption, and stability under various process, voltage, and temperature (PVT) conditions.

- Read and Write Access Times: Compared to radiation-hardened memory cells such as Quatro-10T, RHD-12T, and QCCS-12T, the SEI-14T SRAM cell exhibits faster read and write access times. The SEI-14T is particularly useful for aerospace applications due to its optimized architecture, which reduces latency in both read and write operations.

- Critical Charge: Unlike other radiation-hardened SRAM cells, SEI-14T has a significantly higher critical charge. This means that SEI-14T is less susceptible to radiation-induced disruptions because more energy is required to flip a switch. This is essential to ensure memory cell reliability in high-radiation space applications.

- **Power Consumption:** The SEI-14T SRAM cell exhibits reduced static and dynamic power consumption compared to other designs. This is achieved through careful optimization of the transistor sizes and the overall cell architecture. The reduced power consumption is essential for space applications, where power efficiency is a critical consideration.

- **Stability under PVT Conditions:** The SEI-14T SRAM cell exhibits excellent stability under various PVT conditions. The cell's stability is maintained even under extreme variations in process, voltage, and temperature, ensuring reliable operation in space environments.

Comparison with other radiation-hardened SRAM cells

To overcome the difficulties presented by SEUs and DNUs in space applications, several radiation-hardened SRAM cells have been developed. The Quadro-10T, RHM-12T, RHD-12T, RSP-14T, RH-14T, EDP-12T, and QCCS-12T are some of them. The SEI-14T outperforms these designs in several important areas, including power consumption, read and write stability, and critical charge.

Quatro-10T: The Quatro-10T SRAM cell incorporates a negative feedback recovery latch to improve read stability. However, its critical charge is lower than the SEI-14T, making it more susceptible to radiation-induced disturbances. The SEI-14T offers better stability and error correction capabilities.

RHD-12T: The RHD-12T design features stacked PMOS transistors to reduce read access time and steady-state power consumption. However, it suffers from reduced critical charge at low supply voltages, making it more vulnerable to soft errors. The SEI-14T offers better critical charge and error recovery.

QCCS-12T: Unlike many radiation-hardened memory cells, the QCCS-12T design uses the dual interlocked storage cell (DICE) concept, which provides a higher critical charge. But at lower charge limits, it suffers from soft error recovery failures, while the SEI-14T is not susceptible to them.

4. CONCLUSION AND FUTURE SCOPE

For satellite and space applications, a radiation-hardened RHBD-14T SRAM cell (SEI-14T) has been created that provides resilience against soft errors. Except for the more resilient Q-S0 and QB-S0 edge pairs, SEI-14T memory cells are vulnerable to edge and soft faults. The crucial layout area is deliberately divided to lessen charge-sharing problems. Across a range of PVT situations, SEI-14T exhibits reliable power dissipation and quick write access times. Compared to the QCCS-12T, the SEI-14T offers faster read access times. In addition, its read, write and hold stability are improved under process corner conditions and temperature variations. Additionally, by increasing the critical charge, SEI-14T improves performance in corner cases and VDD variations, which lowers the soft fault rate. Additionally, SEI-14T has high read and write probability and outstanding certification. It provides a strong solution for such vital systems, making it the perfect option for dependable satellite and aeronautical applications.

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