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High-Speed Conditional Bridged Sense Amplifier Flip-Flops for Low-Power Applications

***Meeniga Siva Tarun, K. Vishalakshi**

Sri Sai Institute of Technology and Science, Rayachoty, Andhra Pradesh, India.

*Corresponding Author Email: *meenigasivatarun@gmail.com*

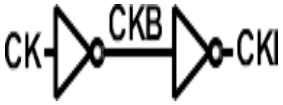
Abstract: *High- Performance issues with typical flip-flops include power consumption at nominal supply voltages and high, erratic performance at low voltages. This study presents conditionally-bridging flip-flops (CBFFs), which have a conditionally-activated shorting device in the sense-amplifier stage, as a solution to these problems. There are two versions a single-ended design is suggested. CBFF-S for low power and area optimization, and a different version CBFF-D targeted at high-speed applications. By activating the shorting device only when needed, CBFFs achieve fully stable operation with reduced switching power. The conditionally-bridging technique reduces parasitic capacitance, simplifies design complexity, and further reduces power. In addition, it enables complete separation of pre-charged nodes during input sampling, supporting fast and reliable operation. The latching state is designed to be jitter-free and contention-free, further reducing latency and power consumption. The CBFF-S, fabricated using a 28-nm CMOS process, shows a 56.2% power saving and a 33.6% delay reduction compared to conventional designs. The CBFF-D achieves up to a 33.8% power reduction and a 24.1% delay improvement. Both designs show an improvement of at least 27.8% in the power-delay product (PDP). Monte Carlo simulations verify that the CBFFs continue to function dependably down to 0.3 V, demonstrating their suitability for near-gate voltage (NTV) applications.*

Keywords: *Flip-flop, low power, low voltage, pulsed latch, sense amplifier and high performance*.

1. INTRODUCTION

Tighter timing requirements and higher clock frequencies are required due to the growing demand for high-speed electronic systems. To meet these requirements, high-speed circuit designs are widely used, especially in performance-critical applications such as mobile systems. Flip-flops and latches in synchronous digital integrated circuits are essential components for managing state changes and making sure info flows in unison. Their performance significantly affects the overall speed and power efficiency of a system, as they are often located in time-critical paths that determine the maximum operating frequency. With millions of flip-flops used in a processor, their combined Power usage may account for 20–40% of the system's overall power. As a result, optimizing flip-flops for minimal power usage and minimal latency is a major challenge in the design of high-speed mobility systems. Conventional transmission-gate flip -flops (TGFFs), with their master-slave structure, offer modest power efficiency and latency. Types such as transmission-gate pulsed latches (TGPLs) improve speed by eliminating the primary state, but suffer from power overhead and reliability issues due to pulse generation complexity and sensitivity to process variations, especially in the area of near-input voltage (NTV). Likewise, flip-flops based on sense amplifiers (SAFFs) achieve high-speed operation through differential pre-charged circuits and symmetrical latching states. However, they suffer from signal contention and increased variability in low-voltage operation due to the weak shorting devices used to ensure stable operation. Attempts to improve SAFF reliability by detecting edge transitions often lead to increased power and delay overhead. To address these limitations, Conditional-bridging flip-flops (CBFFs) are proposed in this study that offer improved speed and reduced power consumption without compromising reliability. The proposed CBFF architecture conditionally implements a shorting device at the step of the sense-amplifier, reducing switching power and reducing parasitic capacitance. This conditional implementation eliminates the need to weaken the shorting device, thus avoiding variation problems in NTV operation. Two variants are introduced: a single-ended design

CBFF-S, optimized for low power and area efficiency, and a differential design CBFF-D, optimized for high-speed performance. Both versions feature jitter-free, contention-free latching states, enabling reliable operation down to 0.3 V. CBFFs eliminate internal clock delay and signal inversion, further reducing latency and power. Performance evaluations in 28-nm CMOS process demonstrate that CBFFs significantly outperform conventional designs in terms of strength, velocity, and energy efficiency. These results highlight how well the suggested conditional bridging method works to accomplish the dual goals of superior performance and energy efficiency in contemporary mobile electronic systems.



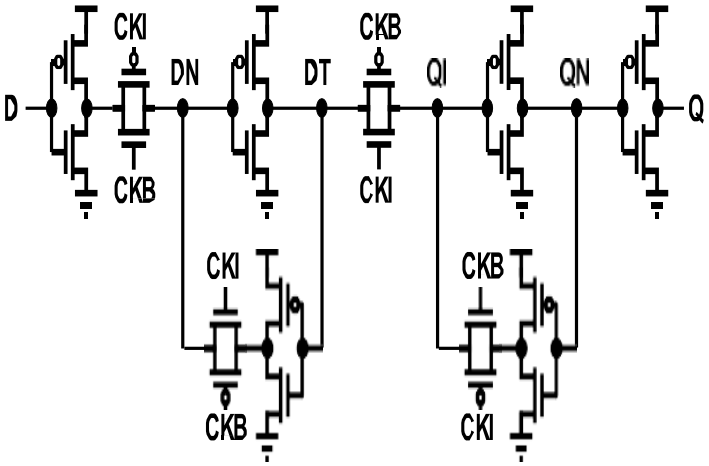


FIGURE 1. TGFF

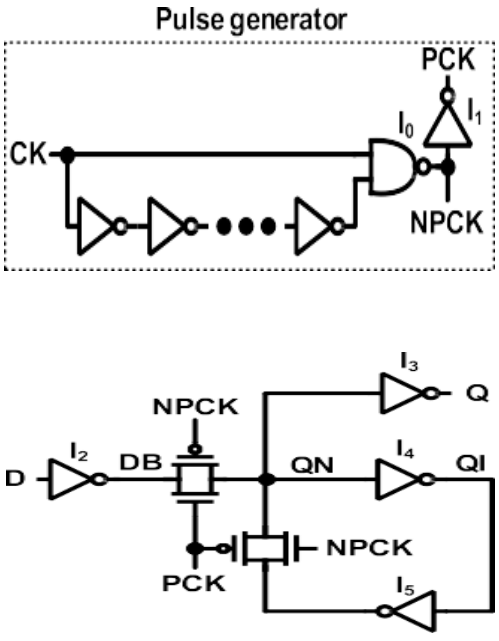


FIGURE 2. Flip-flops based on pulsed latches: TGPL

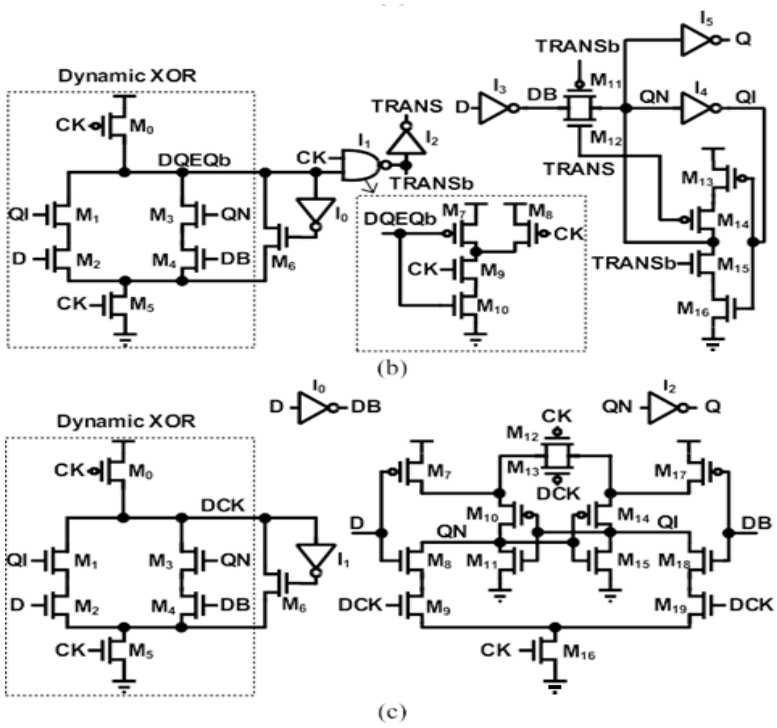


FIGURE 3. Flip-flops based on pulsed latches: (b) STPL and (c) DCP.

2. CONVENTIONAL HIGH-SPEED FLIP-FLOPS

Pulsed latch-based flip-flops

The pulsed latch transmission-gate has a simplified structure with a pulse generator and a single latching stage, which enables reduced DQ latency by directly transferring input data to the internal node during a short clock pulse. However, to ensure reliable operation under worst-case PVT variations, TGPL often requires multiple inverters in the pulse generator, increasing hold time and power consumption. Furthermore, expanding the pulse to improve robustness in near-gate voltage (NTV) regions can lead to increased variability. To address these issues, the self-timed pulsed latch (STPL) uses a dynamic XOR-based pulse generator that generates conditional pulses by detecting changes in the output relative to the input. Although effective in improving timing robustness, STPL suffers from high switching power due to repeated recharge/discharge operations and jitter-induced changes. Furthermore, it may experience operational failures in the NTV region due to race conditions in dynamic logic. The differential feedback pulsed latch (DCPL) addresses the reliability concerns of STPL by ensuring correct signal transitions, but it introduces higher latency and power consumption. Its indirect output pull-up mechanism and repetitive switching behaviour necessitate larger transistors and further increase the switching power. Overall, every design faces trade-offs between speed, power, and reliability, especially under low-voltage conditions.

Sense-amplifier based flip-flops

Figure 3 displays schematic representations of sense-amplifier-based flip-flops (SAFFs). CK being low, SB and RB are replenished in Nikolas's SAFF [17], and the distinct sense-amplifier state models input information on CK's rising edge. Speed is increased by symmetric latching, but the unconditional transitions of SB, RB, and their complements result in increased latency due to high power consumption and inverters in each cycle. The device that reduces M4 between nodes X and Y must be weak for a reliable model, but weakening it increases area, power, and latency. Stromlo's SAFF [18] reduces power and DQ latency by using only SB and RB to drive the symmetric latch, eliminating their complements. However, signal contention during data transitions can increase latency, and increasing transistor sizes to reduce contention results in higher power. The M4 problem also persists. SAFF with transition completion detection (SAFF-TCD) [19] eliminates M4 size concerns by detecting SB and

RB transitions. TC is low during pre-charging, and high after M4 is turned off and pulled up to enable stable operation. However, this approach shows limited improvements in power and latency due to the increased capacitive loads on SB, RB and TC, and the additional latency introduced by NAND requests.

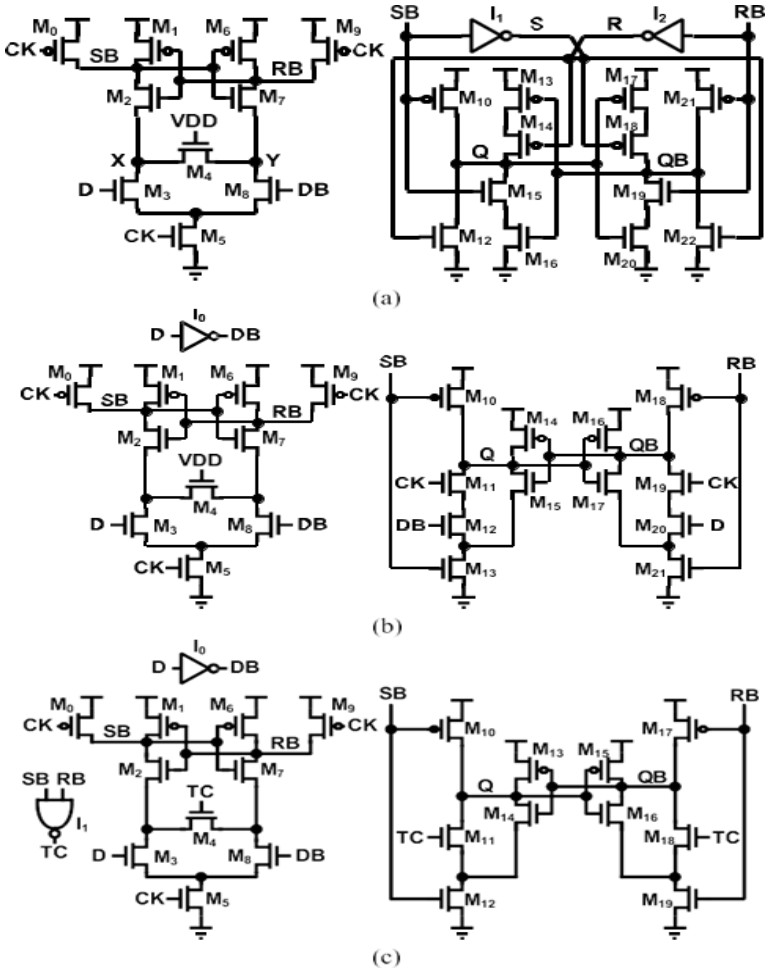


FIGURE 4. Flip-flops utilizing sense amplifiers: (a) Nicholas' SAFF [17], (b) Stroll's SAFF [18], and (c) SAFF-TCD [19].

3. PROPOSED SENSE-AMPLIFIER BASED FLIP-FLOP

Conditional bridge

To more efficiently address the shorting device (M4) issues in conventional SAFFs, an approach of conditional bridging is suggested. It activates M4 only when the input D alters after Q captures it, avoiding unnecessary transitions and unnecessary power consumption. The proposed circuit shown in Figure 4 monitors D, DB, SB, and RB to generate a control signal (CBG) that turns on M4 only when $D \neq Q$ where CK is equal to 1. When CK is low, CBG is low, keeping M4 off. On a rising clock edge, when D changes, CBG goes high, helping to ensure reliable stable operation of M4.

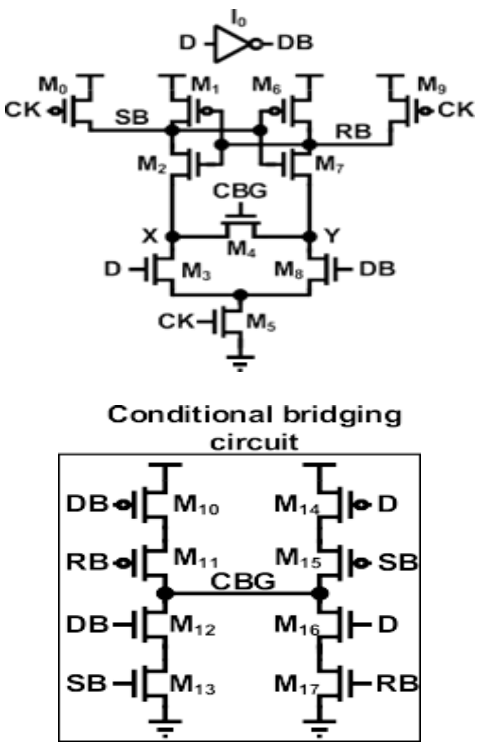


FIGURE 5. Sense amplifier stage incorporating a conditional bridge circuit

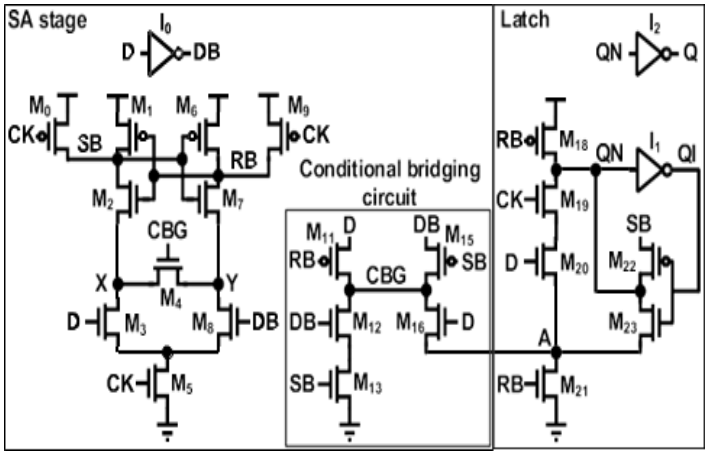


FIGURE 6. Single-ended variant of the proposed flip-flop

Structure and function

The suggested conditional-bridging flip-flop (CBFF) comes in two variants have been developed: a CBFF-S, a single-ended version, and a differential version (CBFF-D). The CBFF-S, shown in Figure 5, includes a stage for a sensory amplifier with a simplified conditional-bridging circuit and a conflict-free latch with one end. The bridging circuit reduces transistor count and power by activating the shorting device (M4) only after D changes after being caught by Q. This eliminates unnecessary switching and allows M4 to be kept to a minimum. The single-ended latch avoids drawbacks and contention by using direct RB control and a selective transistor implementation based on D and SB, ensuring reliable operation even at low supply voltages. The CBFF-S achieves significant power savings, especially under low switching operation, by reducing parasitic capacitance and improving speed through fast pull-down of SB and RB. The CBFF-D, shown in Figure 6, uses a symmetrical differential architecture and shares most of the advantages of the CBFF-S. It reduces the transistor count by combining M13 and M30 and increases the output speed by driving Q and QB directly from SB and RB. A clock transistor (M24) prevents reliability issues related to contention. Although the CBFF-D may consume slightly

more power due to the higher CK load, it outperforms conventional differential flip-flops in power efficiency and speed under low operating conditions.

Typically, Finding the input arrival times that don't capture Q D during the timing sweep is how the setup and hold times are calculated [14].

$$T_{input\_width} = T_{setup} + T_{hold} \quad (1)$$

Here, T_{setup}, T_{hold}, and T_{input_width} represent the minimum necessary input pulse width, the setup time, and the hold duration, in that order. Because the sense-amplifier (SA) stage designs employed for data sampling in the suggested flip-flops and standard SAFFs are similar, these timing characteristics are equivalent.

$$T_{DQ\_min} = min\ \{T_{D-CK}(t_a) + T_{CQ}(t_a)\} \quad (2)$$

$$P_{all} = P_{CH} + P_{SC} + P_{LK} \quad (3)$$

Since P_{CH} and P_{SC} are caused by signal transitions, the suggested conditional bridging method reduces parasitic capacitance at internal nodes and gets rid of pointless transitions leads to a reduction in the suggested flip-flops' total power usage.

4. PERFORMANCE EVALUATION

Utilizing a 28-nm CMOS technology, the proposed and traditional flip-flops utilizing p- and n-type threshold voltages of 0.26V and 0.34V, respectively, to evaluate their performance. Transistor sizes were optimized for power, latency, and area. Parasitic RC values were extracted from the physical design, and Cadence Spectre was used for timing simulations based on these RC-extracted net lists. CQ/DQ and setup/hold time's delays were measured using independent data and clock drivers, buffered by inverters to model realistic transitions. Each flip-flop drove similar FO4 loads in order to assess the velocity. Power elements, such as clock, input, and internal consumption, with the exception of FO4 load switching power - were measured separately using distinct VDD_D, VDD_CK, and VDD_INT provide rails. Configuration and capture times were identified by sweeping the D input transition with 0.1-ps resolution to detect a 10% increase in CQ latency. DQ latency was estimated by measuring the minimum delay from data input to output. Power was estimated under varying input switching functions (e.g., α=0.2 and α=1) using data patterns such as "1111100000…" and "1010101010…" Reliability was verified by 5000 iterations of Monte Carlo simulations across all input, clock, and output transitions; failure to capture data even once was considered unreliable.

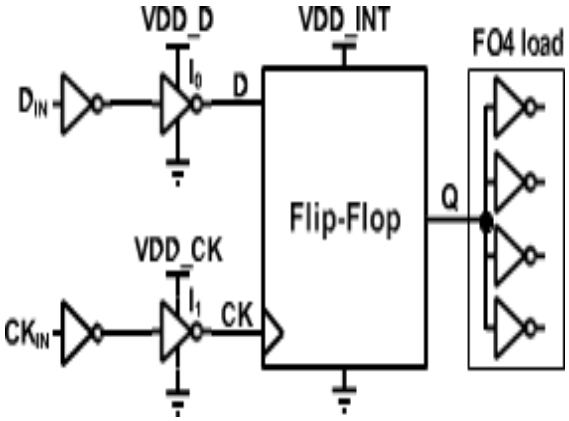


FIGURE 7. Flip-flop simulation environment.

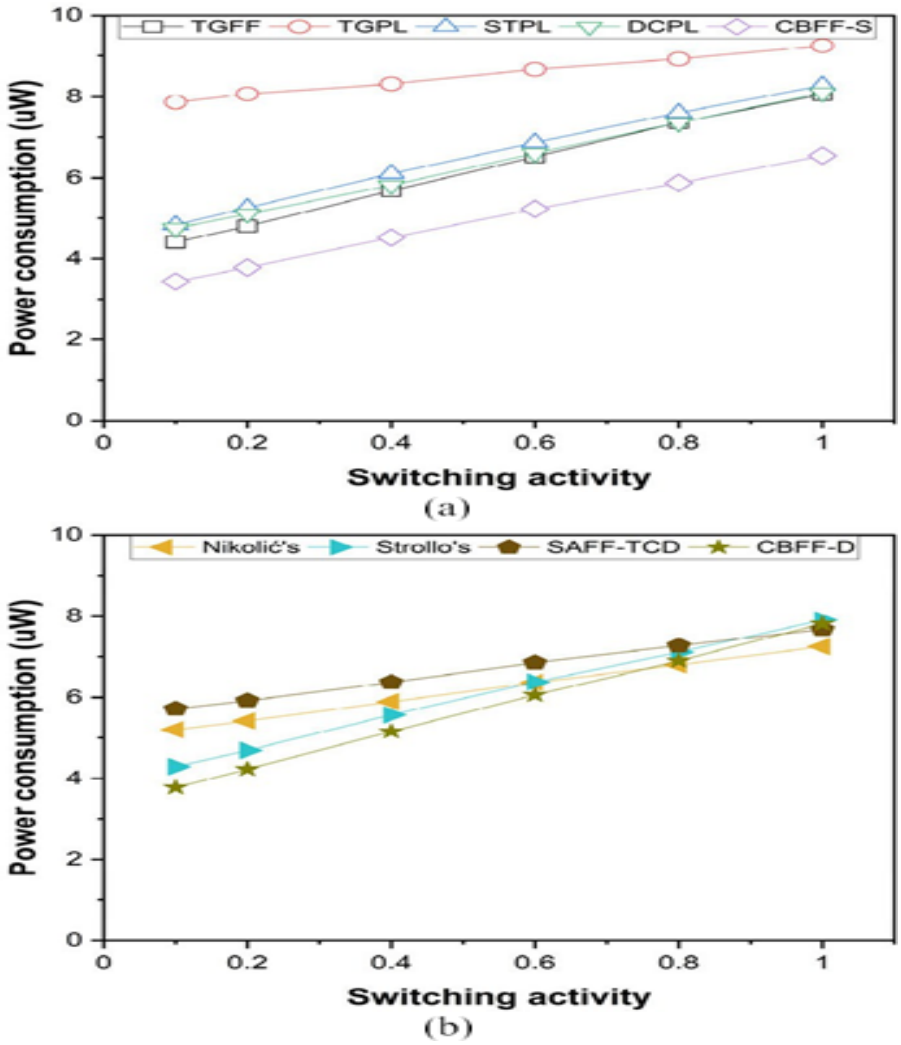


FIGURE 8. Input switching operation and Power consumption for (a) single-ended and (b) differential flip-flops at the TT corner, with a 1-V supply voltage and a temperature of 27°C.

The power consumption of various flip-flops throughout a normal procedure edge (1V, room temperature) for different input switching operations is analysed in Figure 8. For single-ended designs, TGPL shows higher power due to multiple inverters, while STPL and DCPL slightly improve performance. CBFF-S achieves at least 18.7% lower power consumption by replacing power-hungry circuits with a conditionally bridged SA state. In differential designs, CBFF-D significantly reduces power by up to 33.8% in a 0.1 switching operation by eliminating unnecessary transitions and removing inverters and NAND gates, although it slightly increases the clock load. However, CBFF-D offers improved latency compared to conventional differential flip-flops.

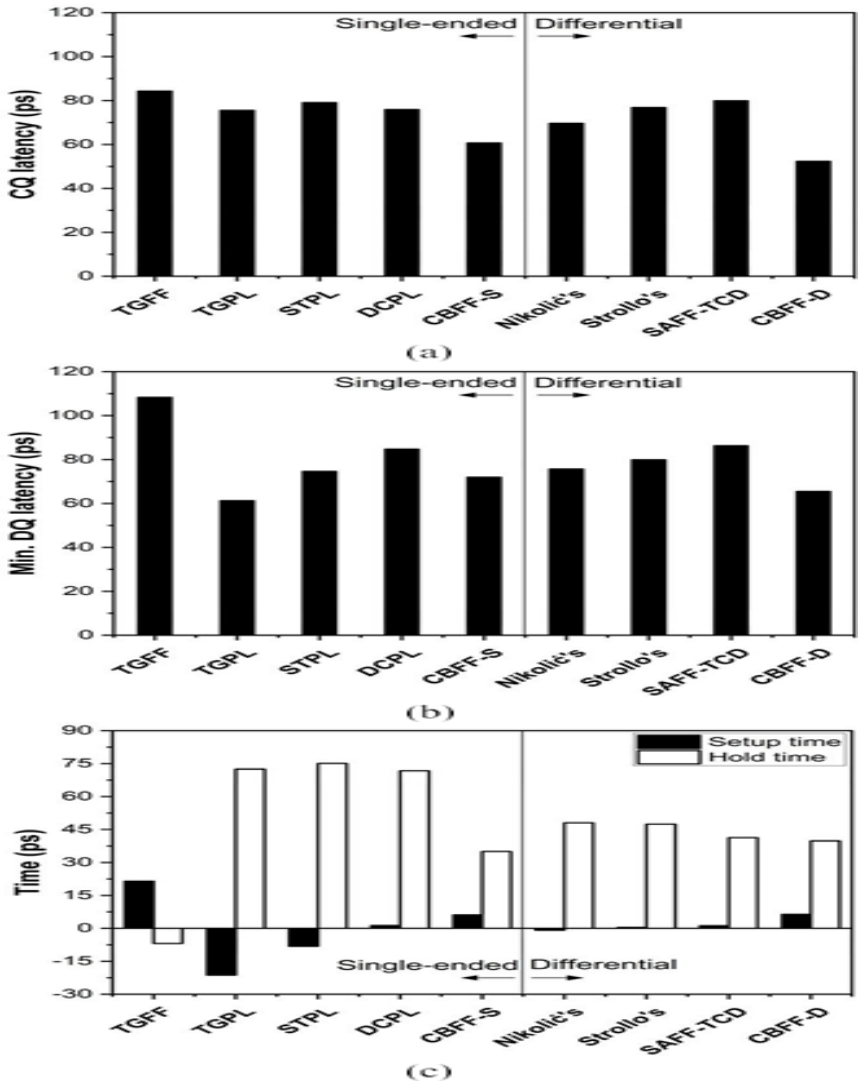


FIGURE 9. Timing performance of flip-flops: (a) CQ delay, (b) minimum DQ delay, and (c) setup and hold times at the TT corner, with a 1-V supply voltage and a temperature of 27°C

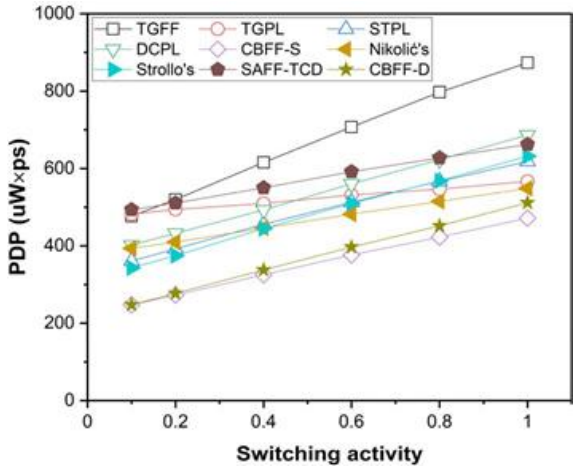


FIGURE 10. Input switching function and power-delay product (PDP) of TT corner flip-flops with a 1-V supply voltage and a temperature of 27°C

VDD(V)	TGFF	TGPL	STPL	DCPL	CBFF-S	Nikolić's SAFF	Strollo's SAFF	SAFF -TCD	CBFF-D
1	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
0.95	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
0.9	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
0.85	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
0.8	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
0.75	PASS	FAIL	PASS	PASS	PASS	FAIL	FAIL	PASS	PASS
0.7	PASS	FAIL	PASS	PASS	PASS	FAIL	FAIL	PASS	PASS
0.65	PASS	FAIL	PASS	PASS	PASS	FAIL	FAIL	PASS	PASS
0.6	PASS	FAIL	PASS	PASS	PASS	FAIL	FAIL	PASS	PASS
0.55	PASS	FAIL	PASS	PASS	PASS	FAIL	FAIL	PASS	PASS
0.5	PASS	FAIL	PASS	PASS	PASS	FAIL	FAIL	PASS	PASS
0.45	PASS	FAIL	FAIL	PASS	PASS	FAIL	FAIL	PASS	PASS
0.4	PASS	FAIL	FAIL	PASS	PASS	FAIL	FAIL	PASS	PASS
0.35	PASS	FAIL	FAIL	PASS	PASS	FAIL	FAIL	PASS	PASS
0.3	FAIL	FAIL	FAIL	FAIL	PASS	FAIL	FAIL	PASS	PASS
0.25	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL

FIGURE 11. Performance of OP flip-flops at measured supply voltages enhanced by #5000 Monte Carlo simulations

The setup/hold timings, minimum DQ delay, and CQ delay Figure 9 shows a comparison of the flip-flops. Figure 9(a) illustrates that CBFFs S and D possess the shortest CQ delays due to the fast SA state pull-up and contention-free latching operation. In terms of minimum DQ delay (Figure 9(b)), CBFF-S outperforms most traditional single-ended flip-flops, with the exception of the TGPL, which has the delay at the expense of higher electricity usage. CBFF-D achieves a minimum DQ delay of up to 24.1% lower than other differential flip-flops. Figure 9(c) shows that CBFFs have shorter positive setup times and shorter hold times than pulse flip-flops, which improves overall performance.

TABLE 1. Comparative performance of flip-flops

	TGPL [13]	STPL [14]	DCPL [15]	**(prop.**	[17]	Strollo's [18]	SAFF-TCD	**(prop.**	[30]	TNVFF [31]
Technology	28-nm CMOS								CNT	
Type	Pulse-based			Sense-amplifier-based					Pulsed	
Output type	Single-ended			Differential						
# of transistors	32	27	26	**27**	29	24	26	**29**	21	
	1	1	1	**1**	1	1	1	**1**	1	0.6
	0.8	0.5	0.34	**0.3**	0.8	0.8	0.3	**0.3**	-	-
	–21.32	–8.17	1.30	**6.13**	–0.87	0.46	1.20	**6.37**	–80	-
(ps	72.5	75.05	71.75	**35.03**	48.06	47.43	41.31	**39.83**	118.2	-
	51.18	66.88	73.06	**41.16**	47.19	47.89	42.51	**46.20**	38.20	-
(p	75.55	79.16	75.91	**60.71**	69.64	76.82	79.93	**52.36**	-	39
	61.28	74.63	84.74	**71.99**	75.70	79.93	86.31	**65.50**	85.17	-

Power consumption @0.1 switching act	7.865	4.831	4.746	**3.439**	5.199	4.292	5.717	**3.781**	0.267	3.8[2)]
Power consumption @0.5 switching act	8.493	6.489	6.214	**4.873**	6.131	5.973	6.614	**5.606**	0.297	
Power consumption @1.0 switching act	9.251	8.279	8.098	**6.552**	7.247	7.904	7.673	**7.812**	0.352	
PDP (μW×ps) @0.1 switching act	481.9	360.5	402.1	**247.6**	393.5	343.06	493.43	**247.6**	22.070	148[2)]
PDP (μW×ps) @0.5 switching ac	520.4	484.2	526.5	**350.8**	464.0	477.38	570.85	**367.1**	25.029	
PDP (μW×ps) @1.0 switching act	566.8	617.8	686.2	**471.6**	548.6	631.77	662.26	**511.6**	29.098	
Layout area (μm	14.19	12.46	12.17	**12.17**	12.95	11.59	11.88	**12.46**	-	-

The data on power and delay in Figures 8 and 9(b) were utilized to calculate the power delay product values are compared in Figure 10. With gains of at least 31.3% and 27.8% at α = 0.1, respectively, All other flip-flops in the single-ended (empty) and differential (filled) categories are outperformed by the PDP of CBFF-S and CBFF-DEven with the highest possible input switching operation, CBFFs still show improvements of 6.7% and 16.7%. PVT Monte Carlo simulations were used to assess the flip-flops' performance at the measured supply voltages variations, as shown in Figure 11. CBFF-S and CBFF-D, like TGFF, DCPL and SAFF-TCD, maintain operation in the NTV region, performing well at voltages down to 0.3V. However, TGPL suffers from pulse-width variation problems, and Nikolic and Strolov's SAFFs are limited to a 0.8-V supply voltage due to device size reduction issues. Although STPL overcomes this problem, its dynamic XOR circuit malfunctions below 0.5 V. In contrast, DCPL operates down to 0.35 V, and CBFFs achieve low-voltage operation by effectively shorting the device size. Table 1 gives an overview of the total performance, noting that TGPL, STPL, and some SAFF designs cannot function within the NTV area. In contrast to flip-flops like DCPL and SAFF-TCD that can function in this area, CBFFs achieve significant reductions in low DQ latency and power usage. This leads to the lowest PDP values of any flip-flop. Although CBFF layout areas are a little bigger than standard flip-flops, their performance improvements make them very attractive for low-power applications. In addition, alternative technologies such as ternary non-volatile flip-flops (TNVFF) and pulse-triggered CNTFET flip-flops (pCNTFF) show better performance than CMOS designs, but face challenges in mass production due to immature manufacturing technologies. Therefore, CMOS-based flip-flops remain a cost-effective and promising solution for large-scale coherent systems. Figure 11 further highlights the advantages within CBFF-S and CBFF-D lowering latency and power consumption, attaining notable PDP gains in comparison to conventional flip-flops.

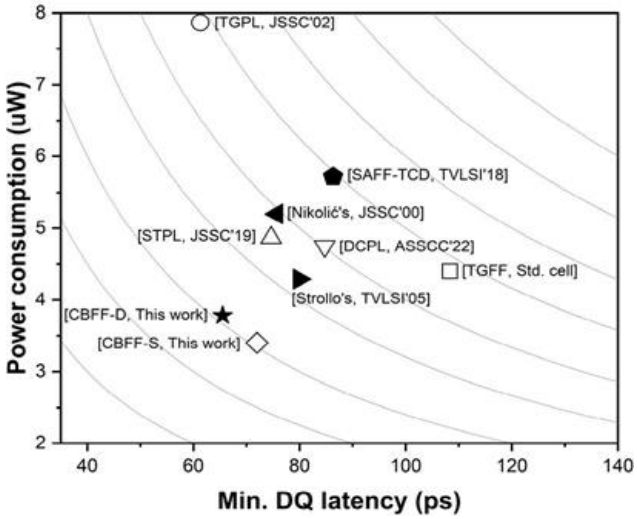


FIGURE 11. Minimum DQ delay and power consumption of single-ended (empty) and differential (filled) flip-flops under 0.1 input TT corner operation, with a 1-V supply voltage and a temperature of 27°C

5. CONCLUSION

This paper introduces flip-flops based on sense amplifiers that are dependable, high-performing, and low-power. The shorting device is implemented adaptively by the suggested conditional bridging technique, guaranteeing steady functioning without unnecessary changes and reducing parasitic capacitance in time-critical paths. Directly driving the latching state without flaws or conflict significantly lowers power consumption and delay. The single-ended version improves power and area with a modified latching state, while the differential version improves speed and supports differential operation. The proposed flip-flops demonstrate reliable operation up to the NTV region, making them appropriate for low-power, high-speed digital applications, as shown in the 28-nm CMOS process evaluation.

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