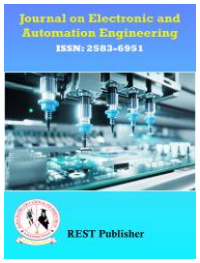
Journal on Electronic and Automation Engineering
Vol: 4(2), June 2025
REST Publisher; ISSN: 2583-6951 (Online)
Website: https://restpublisher.com/journals/jeae/
DOI: https://doi.org/10.46632/jeae/4/2/27



High-Reliability IoT SRAM Architecture Using Nwise and Pwise Cells for Space Applications

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Abstract: *SRAM cells play a critical role in memory components such as caches, register files, and translation lookaside buffers, with their design needing to meet specific requirements based on their intended use. In the aerospace sector, where power efficiency and reliability are paramount due to constrained power resources and exposure to high radiation, the Nwise cell, designed with 28nm FD-SOI technology, addresses these challenges by providing strong reliability and resistance to radiation. This research also presents the Pwise cell, a novel design derived from the Nwise cell and utilizing the same 28nm FD-SOI technology. Simulations indicate that both the Nwise and Pwise cells offer excellent protection against single-event upsets (SEUs) and multiple-event upsets (MEUs) in space environments. The Pwise cell, with its lower read and write latencies, is well-suited for log file applications, while the Nwise cell, with lower read latency and reduced power consumption, is ideal for cache memory designs. Both cells present promising options for space-grade memory systems.*

Index Terms: *28nm FD-SOI technology, cells with Nwise and Pwise configurations, enhanced radiation resistance, durability, multiple-event upsets (MEUs), single-event upsets (SEUs), susceptibility to soft errors, space-focused applications, and the design of SRAM cells.*

1. INTRODUCTION

SRAM cells are fundamental elements in cache memories, register files, and translation lookaside buffers (TLBs), which are integral to the operation of digital processing systems. The performance, dependability, and energy efficiency of these cells have a significant impact on CPU architecture. In the context of aerospace electronics, SRAM cells encounter particular challenges due to exposure to high radiation and the demand for low power consumption. SEUs occur when a charged particle disturbs the data stored in a cell, while MEUs affect multiple nodes at once, potentially leading to system failures. To mitigate these threats, designing radiation-resistant SRAM cells that maintain low latency and power consumption is essential. With the ongoing miniaturization of transistors, ensuring the reliability of these cells becomes increasingly difficult, as smaller transistors are more prone to radiation-induced errors. This challenge has prompted researchers to investigate alternative technologies, such as FD-SOI, which offers better electrostatic control, improved carrier mobility, and reduced leakage current compared to traditional bulk CMOS technology. FD-SOI has demonstrated its effectiveness in minimizing radiation-related damage to SRAM cells, making it particularly suitable for space and aerospace applications. The first section addresses SEU injection modeling in memory cells, the second explores the benefits of FD-SOI over bulk CMOS, and the final section reviews various circuit-level and architectural approaches aimed at enhancing memory system resilience.

$$I(t) = \frac{Q_{dep}}{\tau_f - \tau_r}\left(e^{\frac{-t}{\tau_f}} - e^{\frac{-t}{\tau_r}}\right) \qquad (1)$$

This equation shows that the total charge deposited on the tip, represented as Qdep, results from particle impact in a transient double-layer current source, where τf is the ion-track creation time constant. These time constants are specific to the selected material

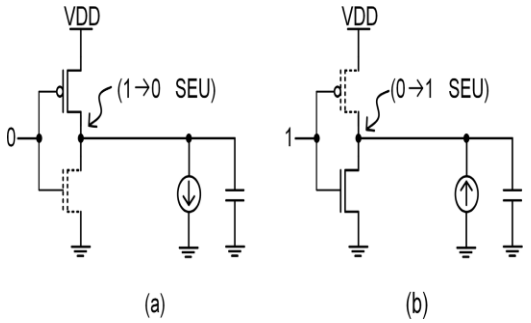

FIGURE 1. Equivalent circuit models designed to simulate (a) noise with a negative injection and (b) noise with a positive injection.

FD-SOI technology improves transistor efficiency by reducing leakage currents and parasitic capacitance, achieved by using a narrow, undoped silicon channel. Though costlier to produce, it offers significant benefits in energy efficiency and radiation resistance, which makes it particularly useful for space-based applications. This research compares different SRAM cells' resistance to radiation, especially under Single Event Upset (SEU) and Multiple Event Upset (MEU) conditions. While traditional designs such as DICE offer strong resilience, they demand larger areas and higher power. On the other hand, the Nwise and Pwise 10T SRAM cells, utilizing 28nm FD-SOI, present a more compact, energy-efficient alternative with reliable recovery from SEU and MEU, making them ideal for use in radiation-sensitive environments, particularly in cache memory.

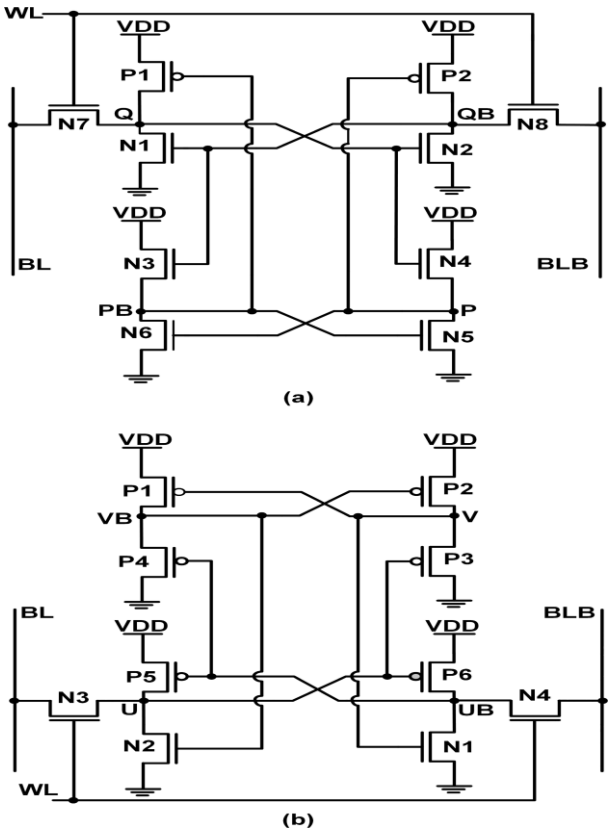

FIGURE 2. The circuit structure of (a) the Nwise cell [55] and (b) the new proposed Pwise cell.

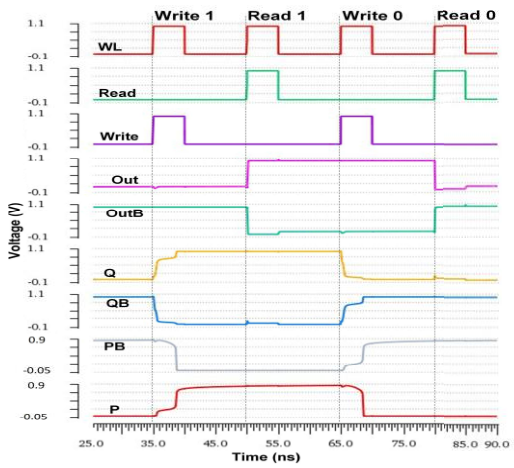

FIGURE 3. The simulation waveform of Nwise cell for a sequential set of operations Write 1, Read 1, Write 0, Read

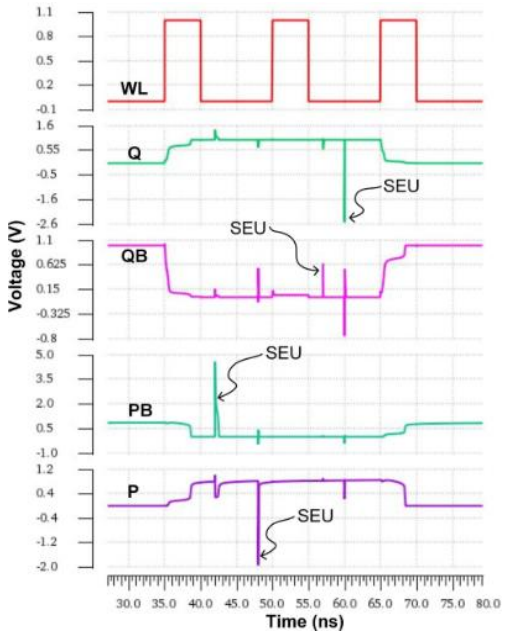

FIGURE 4. SEU tolerance simulation of N wise cell.

When a 1→0 Single Event Upset (SEU) occurs at node Q, transistors N2 and N4 turn off, resulting in floating nodes P and QB. However, this does not affect the stored information, as node PB remains intact. Transistor P1 re-establishes node Q's previous state. Similarly, a 0→1 SEU at node QB is promptly corrected as transistor N2 discharges the node. A 1→0 SEU on node P doesn't impact node PB, ensuring stability. Simulation results confirm that the Nwise cell effectively recovers from SEUs, ensuring data preservation during particle strikes regardless of the SEU's polarity.

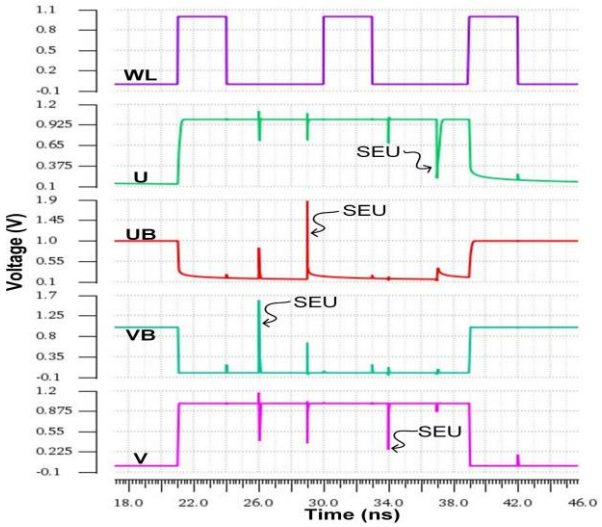

FIGURE 5. SEU tolerance simulation of Pwise cell.

In simulation results are presented for multiple event upset (MEU) tolerance in the Nwise cell, highlighting the behavior of nodes P, Q, and QB under the influence of simultaneous charged particle impacts. As PB remains insensitive, its interactions with other nodes behave similarly to single-event upsets (SEUs). The results demonstrate that the Nwise cell is capable of recovering from multiple impacts on Q, P, and QB within a short time frame, achieving full recovery after each event. At 46ns, simultaneous 1→0 transitions on Q and P lead to recovery, while at 53ns, impacts on QB and P also allow the cell to restore itself. MEUs involving more than two nodes show minimal state changes due to charge diffusion. Moreover, SOI technology enhances MEU resilience by restricting charge collection and coupling. Figure 9 further confirms the similar recovery observed in the Pwise cell, reinforcing the MEU tolerance of both designs.

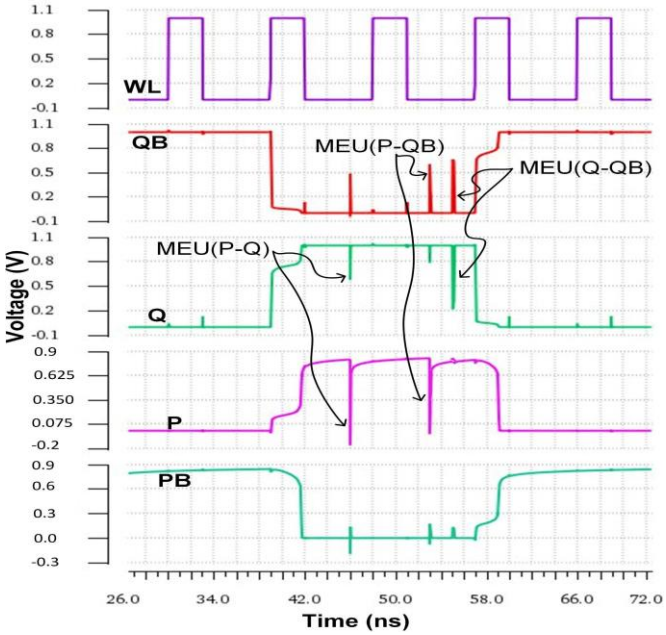

FIGURE 6. MEU tolerance simulation of Nwise cell.

2. DESIGN METHODOLOGY AND SIMULATION RESULTS

To evaluate the performance of the Nwise and Pwise SRAM cells, we conduct a comparison with a range of radiation-hardened designs, such as the 6T SRAM, Quattro, RHBD, NS and PS stacked cells, and the high-speed 10T QUCCE cell. A simulation of a 64-cell SRAM column array is performed under realistic cache memory conditions, incorporating peripheral circuits and signal drivers for a precise assessment. The optimization aims at enhancing robustness, minimizing power consumption, reducing latency, and shrinking area. Transistor dimensions are manually optimized for the best configuration, with layouts created using Cadence Virtuoso and a 28nm FD-SOI process. The simulations deliver key performance metrics, including power usage, latency, noise margins, and area.

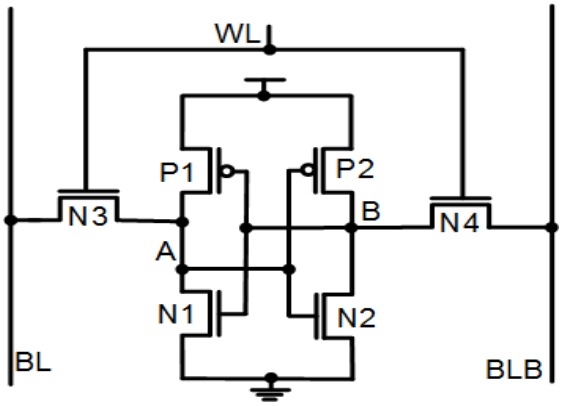

FIGURE 7. The circuit structure of the SRAM_6T cell.

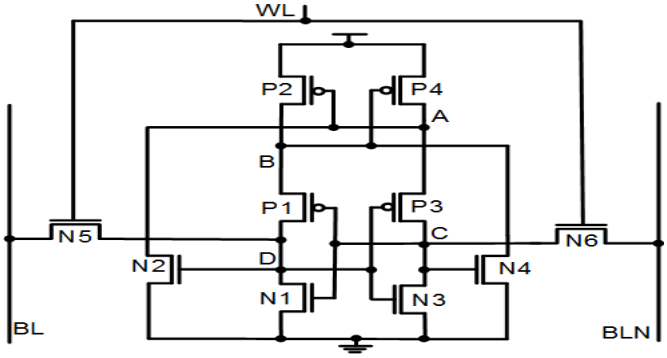

FIGURE 8. Layout view of Nwise cell design.

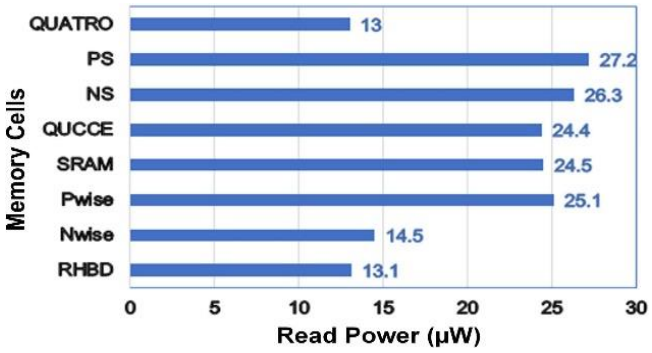

FIGURE 9. Read delay comparisons between all considered cells.

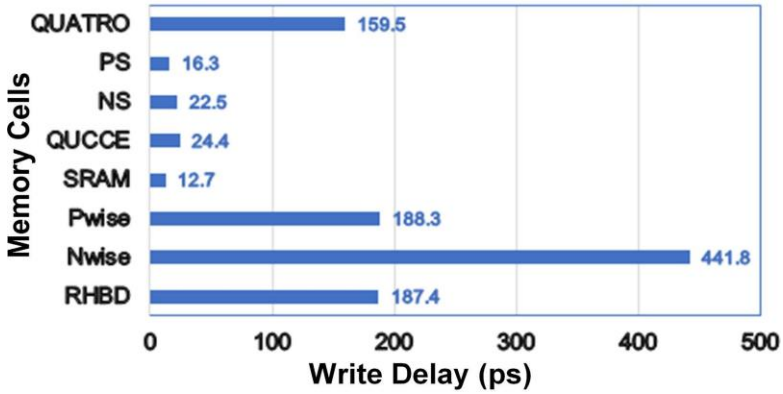

FIGURE 10. Write delay comparisons between all considered cells.

The comparison of access times reveals that the RHBD cell experiences the longest read latency, roughly four times longer than Nwise and nearly three times that of Pwise. This extended latency is due to the multiple activations of PMOS. On the other hand, Nwise suffers from the highest write latency because of feedback overhead. Meanwhile, Pwise strikes a balance, offering superior performance and better SEU tolerance compared to RHBD and Quattro.

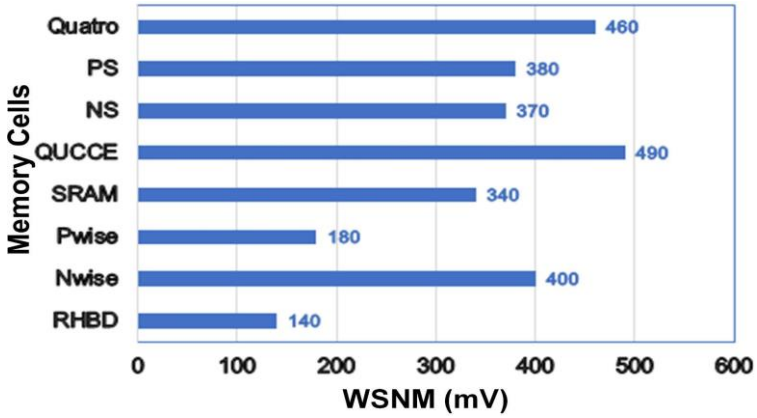

FIGURE 11. WSNM comparisons between all considered cells

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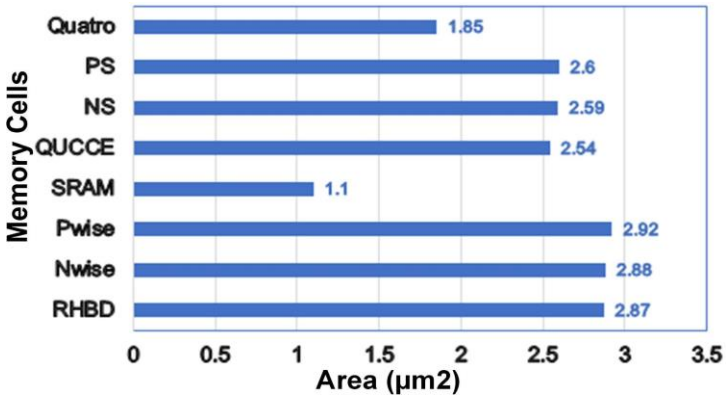

FIGURE 12. Area comparisons between all considered cells.

TABLE 1. Transistor sizes of all tested cells.

	Transistor Sizes
	$W_{P1} = W_{P2} = 200nm, W_{N1} = W_{N2} = 200nm, W_{N3} = W_{N4} = 170nm, W_{N5} = W_{N6} = 80nm, W_{N7} = W_{N8} = 110nm.$
Pwise	$W_{P1} = W_{P2} = 80nm, W_{P3} = W_{P4} = 400nm, W_{P5} = W_{P6} = 300nm, W_{N1} = W_{N2} = 80nm, W_{N3} = W_{N4} = 100nm.$
RHBD [10]	$W_{P1} = W_{P2} = 80nm, W_{P3} = W_{P4} = 200nm, W_{P5} = W_{P6} = 343nm, W_{N1} = W_{N2} = 175nm, W_{N3} = W_{N4} = 100nm.$
Quatro [13]	$W_{P2} = W_{P4} = 120nm, W_{P1} = W_{P3} = 100nm, W_{N2} = W_{N4} = 150nm, W_{N1} = W_{N3} = 200nm, W_{N5} = W_{N6} = 80nm.$
	$W_{P1} = W_{P2} = 100nm, W_{N1} = W_{N2} = 200nm, W_{N3} = W_{N4} = 100nm.$
	$W_{P4} = W_{P2} = 100nm, W_{N4} = W_{N2} = 200nm, W_{N1} = W_{N3} = 150nm, W_{N5} = W_{N6} = 100nm, W_{P3} = W_{P1} = 150nm.$
PS [16]	$W_{P1} = W_{P3} = 100nm, W_{N1} = W_{N3} = 200nm, W_{N2} = W_{N4} = 150nm, W_{N5} = W_{N6} = 100nm, W_{P2} = W_{P4} = 150nm.$
QUCCE [6]	$W_{P1} = W_{P4} = 220nm, W_{P2} = W_{P3} = 80nm, W_{N2} = W_{N3} = 144nm, W_{N1} = W_{N4} 100nm, W_{N5} = W_{N6} = 80nm.$ =

TABLE 2. Cost comparisons for all tested cells.

Cell Name	Write Power (uW)	Read Power (uW)	Write Access Time (ps)	Read Access Time (ps)	WSNM (mV)	RSNM (mV)	HSNM (mV)	Area (um2)	Qcrit (fF)
Nwise	36.1	14.5	27.2	441.8	400	230	390	2.88	0.99
Pwise	30.1	25.1	37.2	188.3	180	270	440	2.92	1
RHBD	18.1	13.1	110.2	187.4	140	180	400	2.87	0.31
	15.1	13	42.8	159.5	460	210	260	1.85	0.97
	22.5	24.5	96.7	12.7	340	150	340	1.1	0.38
NS	24.3	26.3	15.8	22.5	370	150	380	2.59	0.59
PS	25.1	27.2	17.1	16.3	380	140	350	2.6	0.57
QUCCE	24.5	24.4	19.3	24.4	490	180	360	2.54	0.41

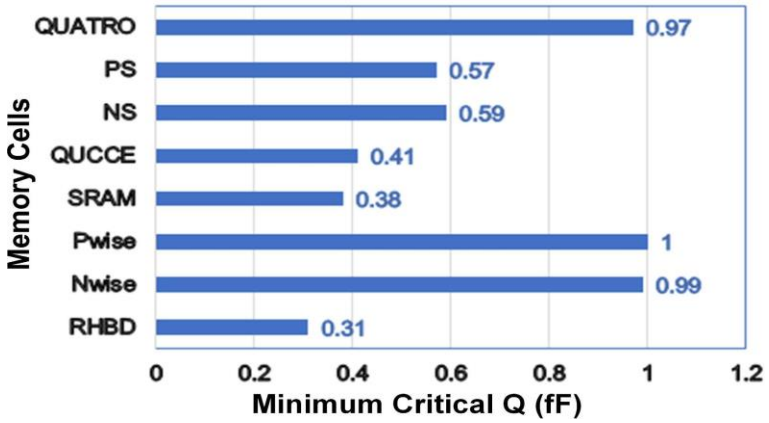

FIGURE 13. Minimum critical charge all considered cells.

The minimum critical charge (Qcrit) across different SRAM cell designs within the temperature range of -55°C to +125°C, typical for aerospace applications. Among the designs evaluated, the Nwise, Quatro, and Pwise cells exhibit the highest Qcrit values at both low and high temperatures. The temperature-dependent variation in Qcrit is 0.15 fF for Nwise, 0.16 fF for Quatro, and 0.62 fF for Pwise. However, the Quatro design is unsuitable for extreme environments, as it fails to provide full protection against single-event upsets (SEUs). As a result, both Nwise and Pwise cells retain the highest Qcrit values throughout the temperature spectrum, offering superior resistance to multiple-event upsets (MEUs) compared to the other configurations.

3. DISCUSSION

I notice you've sent an incomplete sentence. You mentioned "Table 2 presents a cost comparison of the evaluated SRAM cells. The Nwise" but didn't complete the thought and Pwise designs feature the highest critical node capacitances, which directly increases their cost. These elevated capacitances result from the transistors in their feedback circuits that enhance radiation resilience, as detailed in Section IV-A5. Although Quattro lacks complete SEU immunity, it shows comparable costs to the Nwise and Pwise cells. Both Nwise and Pwise incorporate two pairs of cross-coupled transistors (NMOS and PMOS) along with feedback pathways that increase capacitance. The cost variations between these cells are influenced by transistor dimensions; specifically, the Nwise cell's additional feedback transistors contribute to its longer writing delay.

4. CONCLUSION

The Poise cell represents an advanced radiation-hardened SRAM design implemented in 28nm FD-SOI technology, building upon principles from our previously introduced Noise cell. Our research includes comprehensive simulation analysis comparing Nowise and Poise cells against other radiation-hardened SRAM designs intended for space application memory systems. These designs exhibit excellent resilience against single-event upsets (SEUs) and show strong tolerance to multiple-event upsets (MEUs) across the temperature variations commonly encountered in space. The Noise cell stands out with its lower read delay and reduced power consumption when compared to other designs with similar radiation resistance, positioning it as an ideal candidate for cache memory implementations Meanwhile, the Pwise cell's minimal read and write latencies make it more appropriate for register file implementations.

REFERENCES

[1]. L. J. Hennessy and D. A. Patterson, Computer Architecture: A Quantitative Approach, 5th ed. San Francisco, CA, USA: Morgan Kaufmann, 2011.

[2]. M. A. Bajura, Y. Boulghassoul, R. Naseer, S. DasGupta, A. F. Witulski, J. Sondeen, S. D. Stansberry, J. Draper, L. W. Massengill, and J. N. Damoulakis, ‘‘Models and algorithmic limits for an ECC-based approach to hardening sub-100-nm SRAMs,’’ IEEE Trans. Nucl. Sci., vol. 54, no. 4, pp. 935–945, Aug. 2007.

[3]. J. Teifel, ‘‘Self-voting dual-modular-redundancy circuits for single- event-transient mitigation,’’ IEEE Trans. Nucl. Sci., vol. 55, no. 6, pp. 3435–3439, Dec. 2008.

[4]. L. Sterpone and M. Violante, ‘‘Analysis of the robustness of the TMR architecture in SRAM-based FPGAs,’’ IEEE Trans. Nucl. Sci., vol. 52, no. 5, pp. 1545–1549, Oct. 2005.

[5]. R. Giterman, L. Atias, and A. Teman, ‘‘Area and energy-efficient com- plementary dual-modular redundancy dynamic memory for space applica- tions,’’ IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 2, pp. 502–509, Feb. 2017.

[6]. J. Jiang, Y. Xu, W. Zhu, J. Xiao, and S. Zou, ‘‘Quadruple cross-coupled latch-based 10T and 12T SRAM bit-cell designs for highly reliable terres- trial applications,’’ IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 66, no. 3, pp. 967–977, Mar. 2019.

[7]. K. C. Mohr and L. T. Clark, ‘‘Delay and area efficient first-level cache soft error detection and correction,’’ in Proc. Int. Conf. Comput. Design, Oct. 2006, pp. 88–92.

[8]. T. Calin, M. Nicolaidis, and R. Velazco, ‘‘Upset hardened memory design for submicron CMOS technology,’’ IEEE Trans. Nucl. Sci., vol. 43, no. 6, pp. 2874–2878, Dec. 1996.

[9]. D. Lin, Y. Xu, X. Liu, W. Zhu, L. Dai, M. Zhang, X. Li, X. Xie, J. Jiang, H. Zhu, Z. Zhang, and S. Zou, ‘‘A novel highly reliable and low-power radiation hardened SRAM bit-cell design,’’ IEICE Electron. Exp., vol. 15, no. 3, Feb. 2018, Art. no. 20171129.

[10]. J. Guo, L. Zhu, Y. Sun, H. Cao, H. Huang, T. Wang, C. Qi, R. Zhang, X. Cao, L. Xiao, and Z. Mao, ‘‘Design of area-efficient and highly reliable RHBD 10T memory cell for aerospace applications,’’ IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 26, no. 5, pp. 991–994, May 2018.

[11]. C. Peng, Z. Chen, J. Zhang, S. Xiao, C. Liu, X. Wu, and Z. Lin, ‘‘A radiation harden enhanced quatro (RHEQ) SRAM cell,’’ IEICE Electron. Exp., vol. 14, no. 18, 2017, Art. no. 20170784.

[12]. O. Chertkow, A. Pescovsky, L. Atias, and A. Fish, ‘‘A novel low power bitcell design featuring inherent SEU prevention and self correction capabilities,’’ J. Low Power Electron. Appl., vol. 5, no. 2, pp. 130–150, Jun. 2015.

[13]. S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev, "A soft error tolerant 10T SRAM bit-cell with differential read capability," IEEE Trans. Nucl. Sci., vol. 56, no. 6, pp. 3768–3773, Dec. 2009.

[14]. C. Qi, L. Xiao, T. Wang, J. Li, and L. Li, "A highly reliable memory cell design combined with layout-level approach to tolerant single-event upsets," IEEE Trans. Device Mater. Rel., vol. 16, no. 3, pp. 388–395, Sep. 2016.

[15]. L. D. T. Dang, J. S. Kim, and I. J. Chang, "We-quatro: Radiation-hardened SRAM cell with parametric process variation tolerance," IEEE Trans. Nucl. Sci., vol. 64, no. 9, pp. 2489–2496, Sep. 2017.

[16]. I.-S. Jung, Y.-B. Kim, and F. Lombardi, "A novel sort error hardened 10T SRAM cells for low voltage operation," in Proc. IEEE 55th Int. Midwest Symp. Circuits Syst. (MWSCAS), Aug. 2012, pp. 714–717.

[17]. J. Guo, L. Xiao, T. Wang, S. Liu, X. Wang, and Z. Mao, "Soft error hardened memory design for nanoscale complementary metal oxide semi- conductor technology," IEEE Trans. Rel., vol. 64, no. 2, pp. 596–602, Jun. 2015.

[18]. J. Guo, L. Xiao, and Z. Mao, "Novel low-power and highly reliable radi- ation hardened memory cell for 65 nm CMOS technology," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 7, pp. 1994–2001, Jul. 2014.

[19]. S. Lin, Y.-B. Kim, and F. Lombardi, "Analysis and design of nanoscale CMOS storage elements for single-event hardening with multiple-node upset," IEEE Trans. Device Mater. Rel., vol. 12, no. 1, pp. 68–77, Mar. 2012.

[20]. S. Lin, Y. Kim, and F. Lombardi, "A 11-transistor nanoscale CMOS memory cell for hardening to soft errors," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 5, pp. 900–904, May 2011.

[21]. R. Rajaei, B. Asgari, M. Tabandeh, and M. Fazeli, "Design of robust SRAM cells against single-event multiple effects for nanometer tech- nologies," IEEE Trans. Device Mater. Rel., vol. 15, no. 3, pp. 429–436, Sep. 2015.

[22]. J. Karp, W. Regitz, and S. Chou, "A 4096-bit dynamic MOS RAM," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 1972, pp. 10–11.

[23]. N. Ikeda, T. Terano, H. Moriya, T. Emori, and T. Kobayashi, "A novel logic compatible gain cell with two transistors and one capacitor," in Symp. VLSI Technol. Dig. Tech. Papers, 2000, pp. 168–169.

[24]. K. C. Chun, P. Jain, T.-H. Kim, and C. H. Kim, "A 667 MHz logic- compatible embedded DRAM featuring an asymmetric 2T gain cell for high speed on-die caches," IEEE J. Solid-State Circuits, vol. 47, no. 2, pp. 547–559, Feb. 2012.

[25]. R. Giterman, A. Fish, N. Geuli, E. Mentovich, A. Burg, and A. Teman, "An 800-MHz mixed-VT 4T IFGC embedded DRAM in 28-nm CMOS bulk process for approximate storage applications," IEEE J. Solid-State Circuits, vol. 53, no. 7, pp. 2136–2148, Jul. 2018.

[26]. P. Meinerzhagen, A. Teman, R. Giterman, N. Edri, A. Burg, and A. Fish, Gain-Cell Embedded DRAMs for Low-Power VLSI Systems-on-Chip. Basel, Switzerland: Springer, 2018.

[27]. R. Giterman, A. Teman, P. Meinerzhagen, A. Burg, and A. Fish, "4T gain-cell with internal-feedback for ultra-low retention power at scaled CMOS nodes," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), Jun. 2014, pp. 2177–2180.

[28]. L. Atias, A. Teman, R. Giterman, P. Meinerzhagen, and A. Fish, "A low- voltage radiation-hardened 13T SRAM bitcell for ultralow power space applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 8, pp. 2622–2633, Aug. 2016.

[29]. C. Qi, L. Xiao, M. Huo, T. Wang, R. Zhang, and X. Cao, "A 13T radiation- hardened memory cell for low-voltage operation and ultra-low power space applications," in Proc. 18th Int. Symp. Quality Electron. Design (ISQED), Mar. 2017, pp. 161–165.

[30]. N. Verma and A. P. Chandrakasan, "A 256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy," IEEE J. Solid-State Cir- cuits, vol. 43, no. 1, pp. 141–149, Jan. 2008.

[31]. C. Peng, "Radiation-hardened 14T SRAM bitcell with speed and power optimized for space application," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 27, no. 2, pp. 407–415, Nov. 2019.

[32]. A. Yan, Z. Wu, J. Guo, J. Song, and X. Wen, "Novel double-node-upset- tolerant memory cell designs through radiation-hardening-by-design and layout," IEEE Trans. Rel., vol. 68, no. 1, pp. 354–363, Mar. 2019.

[33]. Y. Han, X. Cheng, J. Han, and X. Zeng, "Radiation-hardened 0.3–0.9-V voltage-scalable 14T SRAM and peripheral circuit in 28-nm technology for space applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 28, no. 4, pp. 1089–1093, Apr. 2020.

[34]. C. N. Raghuram, B. Gupta, and G. Kaushal, "Double node upset tolerant RHBD15T SRAM cell design for space applications," IEEE Trans. Device Mater. Rel., vol. 20, no. 1, pp. 181–190, Mar. 2020.

[35]. C. I. Kumar and B. Anand, "A highly reliable and energy efficient radiation hardened 12T SRAM cell design," IEEE Trans. Device Mater. Rel., vol. 20, no. 1, pp. 58–66, Mar. 2020.

[36]. L. Wen, Y. Zhang, and P. Wang, "Radiation-hardened, read-disturbance- free new-quatro-10T memory cell for aerospace applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 28, no. 8, pp. 1935–1939, Aug. 2020.

[37]. Q. Zhao, C. Peng, J. Chen, Z. Lin, and X. Wu, "Novel write-enhanced and highly reliable RHPD-12T SRAM cells for space applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 28, no. 3, pp. 848–852, Mar. 2020.

[38]. J. Guo, L. Zhu, W. Liu, H. Huang, S. Liu, T. Wang, L. Xiao, and Z. Mao, ‘‘Novel radiation-hardened-by-design (RHBD) 12T memory cell for aerospace applications in nanoscale CMOS technology,’’ IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 5, pp. 1593–1600, May 2017.

[39]. D. Truyen, E. Leduc, and F. Braud, ‘‘Elimination of single event latch-up in the ATMEL ATMX150RHA rad-hard CMOS 150 nm cell-based ASIC family,’’ in Proc. 15th Eur. Conf. Radiat. Effects Compon. Syst. (RADECS), Sep. 2015, pp. 1–3.

[40]. G. C. Messenger, ‘‘Collection of charge on junction nodes from ion tracks,’’ IEEE Trans. Nucl. Sci., vol. NS-29, no. 6, pp. 2024–2031, Dec. 1982.

[41]. V. Malherbe, G. Gasiot, D. Soussan, J.-L. Autran, and P. Roche, ‘‘On-orbit upset rate prediction at advanced technology nodes: A 28 nm FD-SOI case study,’’ IEEE Trans. Nucl. Sci., vol. 64, no. 1, pp. 449–456, Jan. 2017.

[42]. (Apr. 2014). Amiad Conley, FinFET vs. FD-SOI Key Advantages & Dis- advantages, ChipEx-2014. Accessed: Mar. 9, 2022. [Online]. Available: http://www.chipex.co.il/_Uploads/dbsAttachedFiles/ChipExAMAT.pdf

[43]. Bulk CMOS Vs. FD-SOI. Accessed: Mar. 9, 2022. [Online]. Available: https://semiengineering.com/bulk-cmos-versus-fd-soi/

[44]. J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits—A Design Perspective. Upper Saddle River, NJ, USA: Prentice-Hall, 2004.

[45]. H. Cha and J. H. Patel, ‘‘A logic-level model for α-particle hits in CMOS circuits,’’ in Proc. IEEE Int. Conf. Comput. Design (ICCD), Oct. 1993, pp. 538–542.

[46]. N. H. E. Weste and D. M. Harris, CMOS VLSI Design: A Circuits and Systems Perspective. Boston, MA, USA: Pearson, 2005.

[47]. G. E. Moore, ‘‘Cramming more components onto integrated circuits,’’ Electronics, vol. 38, no. 8, pp. 114–117, Apr. 1965.

[48]. P. Vargas, ‘‘Evaluation of the SEE sensitivity and methodology for error rate prediction of applications implemented in multi-core and many-core processors,’’ Ph.D. dissertation, Univ. Grenoble Alpes, Grenoble, France, Apr. 2017.

[49]. A. Seyedi, A. Armejach, A. Cristal, O. S. Unsal, I. Hur, and M. Valero, ‘‘Circuit design of a dual-versioning L1 data cache for optimistic con- currency,’’ in Proc. 21st, Ed., Great Lakes Symp. Great lakes Symp. VLSI (GLSVLSI), 2011, pp. 325–350.

[50]. A. Seyedi, A. Armejach, A. Cristal, O. S. Unsal, I. Hur, and M. Valero, ‘‘Circuit design of a dual-versioning L1 data cache,’’ Integration, vol. 45, no. 3, pp. 237–245, Jun. 2012.

[51]. H.-H.-K. Lee, L. Klas, B. Mounaim, R. Prasanthi, I. R. Linscott, U. S. Inan, and M. Subhasish, ‘‘LEAP: Layout design through error-aware transistor positioning for soft-error resilient sequential cell design,’’ in Proc. IEEE Int. Rel. Phys. Symp., May 2010, pp. 203–212.

[52]. E. Seevinck, F. J. List, and J. Lohstroh, ‘‘Static-noise margin analysis of MOS SRAM cells,’’ IEEE J. Solid-State Circuits, vol. SSC-22, no. 5, pp. 748–754, Oct. 1987.

[53]. A. Seyedi, A. Armejach, A. Cristal, O. S. Unsal, and M. Valero, ‘‘Novel SRAM bias control circuits for a low power L1 data cache,’’ in Proc. NORCHIP, Nov. 2012, pp. 1–6.

[54]. A. Armejach, A. Seyedi, R. Titos-Gil, I. Hur, A. Cristal, O. S. Unsal, and M. Valero, ‘‘Using a reconfigurable L1 data cache for efficient version management in hardware transactional memory,’’ in Proc. Int. Conf. Par- allel Architectures Compilation Techn., Oct. 2011, pp. 361–371.

[55]. A. Seyedi, S. Aunet, and P. G. Kjeldsberg, ‘‘Nwise: An area efficient and highly reliable radiation hardened memory cell designed for space appli- cations,’’ in Proc. IEEE Nordic Circuits Syst. Conf. (NORCAS), NORCHIP Int. Symp. Syst.-Chip (SoC), Oct. 2019, pp. 1–6.

[56]. A. Makihara, T. Yamaguchi, H. Asai, Y. Tsuchiya, Y. Amano, M. Midorikawa, H. Shindou, S. Onoda, T. Hirao, Y. Nakajima, T. Takahashi, K. Ohnishi, and S. Kuboyama, ‘‘Optimization for SEU/SET immunity on 0.15 µm fully depleted CMOS/SOI digital logic devices,’’ IEEE Trans. Nucl. Sci., vol. 53, no. 6, pp. 3422–3427, Dec. 2006.

[57]. J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, and P. E. Dodd, ‘‘Radiation effects in SOI technologies,’’ IEEE Trans. Nucl. Sci., vol. 50, no. 3, pp. 522–538, Jun. 2003.

[58]. Y. Kuang, J. Bu, B. Li, L. Gao, C. Liang, Z. Han, and J. Luo, ‘‘Total dose effects of 28 nm FD-SOI CMOS transistors,’’ in Proc. IEEE SOI- 3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S), Oct. 2018, pp. 1–3.

[59]. M. L. Alles, D. R. Ball, L. W. Massengill, R. D. Schrimpf, R. A. Reed, and B. L. Bhuva, ‘‘Scaling and soft errors: Moore of the same for SOI ?’’ in Proc. IEEE Int. SOI Conf., Oct. 2008, pp. 129–130.

[60]. R. D. Schrimpf, M. L. Alles, D. M. Fleetwood, D. R. Ball, M. J. Gadlage, and F. El Mamouni, ‘‘Design and evaluation of SOI devices for radi- ation environments,’’ in Proc. IEEE Int. SOI Conf. (SOI), Oct. 2010, pp. 1–4.

[61]. E. H. Cannon, M. S. Gordon, D. F. Heidel, A. J. KleinOsowski, P. Oldiges, K. P. Rodbell, and H. H. K. Tang, ‘‘Multi-bit upsets in 65 nm SOI SRAMs,’’ in Proc. IEEE Int. Rel. Phys. Symp., Apr. 2008, pp. 195–201.

[62]. F. L. Yang and R. A. Saleh, ‘‘Simulation and analysis of transient faults in digital circuits,’’ IEEE J. Solid-State Circuits, vol. 27, no. 3, pp. 258–264, Mar. 1992.

[63]. H. Nan and K. Choi, ‘‘High performance, low cost, and robust soft error tolerant latch designs for nanoscale CMOS technology,’’ IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 7, pp. 1445–1457, Jan. 2012.

[64]. D. R. Blum and J. G. Delgado-Frias, ‘‘Hardened by design techniques for implementing multiple-bit upset tolerant static memories,’’ in Proc. IEEE Int. Symp. Circuits Syst., May 2007, pp. 2786–2789.

[65]. B. Pelloux-Prayer, M. Blagojevic, S. Haendler, A. Valentian, A. Amara, and P. Flatresse, ‘‘Performance analysis of multi-VT design solutions in 28 nm UTBB FD-SOI technology,’’ in Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S), Oct. 2013, pp. 1–2.

[66]. H. Mori, T. Nakagawa, Y. Kitahara, Y. Kawamoto, K. Takagi, S. Yoshimoto, S. Izumi, H. Kawaguchi, and M. Yoshimoto, ‘‘A 28-nm FD-SOI 8T dual-port SRAM for low-energy image processor with selec- tive sourceline drive scheme,’’ IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 66, no. 4, pp. 1442–1453, Apr. 2019.

[67]. Cactus Technologies, Commercial and Industrial-Grade Products, White Paper CTWP011. Accessed: Mar. 9, 2022. [Online]. Available: https://www.cactus-tech.com/wpcontent/uploads/2019/03/Commercial- and-Industrial-Grade-Products.pdf

[68]. Maxim Integrated, IC Applications in Aerospace and Defense. Accessed: Mar. 9, 2022. [Online]. Available: https://www.maximintegrated.com/en/applications/aerospacedefense.html

[69]. Military Operating Temperature. Accessed: Mar. 9, 2022. [Online]. Avail- able: https://en.wikipedia.org/wiki/Operating_temperature

[70]. S. Lin, Y.-B. Kim, and F. Lombardi, ‘‘Modeling and design of a nanoscale memory cell for hardening to a single event with multiple node upset,’’ in Proc. IEEE 29th Int. Conf. Comput. Design (ICCD), Oct. 2011, pp. 320–325.

[71]. FD-SOI. Accessed: Mar. 9, 2022. [Online]. Available: https://www.st.com/content/st_com/en/about/innovation—technology/ FD-SOI.html

[72]. H. Ahangari, I. Alouani, O. Ozturk, S. Niar, and A. Rivenq, ‘‘Register file reliability enhancement through adjacent narrow-width exploitation,’’ in Proc. Int. Conf. Design Technol. Integr. Syst. Nanosc. Era (DTIS), Apr. 2016, pp. 1–4.

[73]. I. Carlson, ‘‘Design and evaluation of high density 5T SRAM cache for advanced microprocessors,’’ Linkoping Univ., Linköping, Sweden, Tech. Rep. LiTH-ISY-EX-3481-2004, 2004.

[74]. G. Prasad, B. C. Mandi, and M. Ali, ‘‘Power optimized SRAM cell with high radiation hardened for aerospace applications,’’ Microelectron. J., vol. 103, Sep. 2020, Art. no. 104843.

[75]. S. Pal, D. D. Sri, W.-H. Ki, and A. Islam, ‘‘Soft-error resilient read decoupled SRAM with multi-node upset recovery for space applications,’’ IEEE Trans. Electron Devices, vol. 68, no. 5, pp. 2246–2254, May 2021.

[76]. S. Pal, D. D. Sri, W.-H. Ki, and A. Islam, ‘‘Highly stable low power radiation hardened memory-by-design SRAM for space applications,’’ IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 68, no. 6, pp. 2147–2151, Jun. 2021.

[77]. S. Pal, S. Mohapatra, W.-H. Ki, and A. Islam, ‘‘Soft-error-aware read- decoupled SRAM with multi-node recovery for aerospace applications,’’ IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 68, no. 10, pp. 3336–3340, Oct. 2021.

[78]. S. Pal, S. Mohapatra, W.-H. Ki, and A. Islam, ‘‘Design of soft-error- aware SRAM with multi-node upset recovery for aerospace applications,’’ IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 68, no. 6, pp. 2470–2480, Jun. 2021.

[79]. S. Pal, S. Mohapatra, W.-H. Ki, and A. Islam, ‘‘Soft-error-immune read- stability-improved SRAM for multi-node upset tolerance in space appli- cations,’’ IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 68, no. 8, pp. 3317–3327, Aug. 2021.

[80]. [80] S. S. Dohar, R. K. Siddharth, M. H. Vasantha, and Y. B. N. Kumar, ‘‘A 1.2 V, highly reliable RHBD 10T SRAM cell for aerospace application,’’ IEEE Trans. Electron Devices, vol. 68, no. 5, pp. 2265–2270, May 2021.

[81]. Y. Han, T. Li, X. Cheng, L. Wang, J. Han, Y. Zhao, and X. Zeng, ‘‘Radiation hardened 12T SRAM with crossbar-based peripheral circuit in 28 nm CMOS technology,’’ IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 68, no. 7, pp. 2962–2975, Jul. 2021.

[82]. N. R. Ch, B. Gupta, and G. Kaushal, ‘‘Single-event multiple effect tolerant RHBD14T SRAM cell design for space applications,’’ IEEE Trans. Device Mater. Rel., vol. 21, no. 1, pp. 48–56, Mar. 2021.

[83]. H. Li, L. Xiao, C. Qi, and J. Li, ‘‘Design of high-reliability memory cell to mitigate single event multiple node upsets,’’ IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 68, no. 10, pp. 4170–4181, Oct. 2021.