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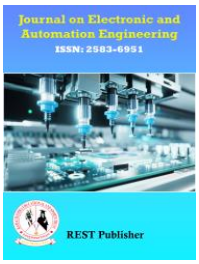

Exploration of CNTFET-Oriented Approximate Full Adders: Techniques, Challenges, and Future Prospects

Sushmitha A. K, Geethanjali D, Riyaz D, Prathyusha B, *Dasamandam Venkata Supriya

Annamacharya Institute of Technology & Science (AITK), Kadapa, Andhra Pradesh, India
**Corresponding Author Email*: venkata.supriya8@gmail.com.

Abstract: *Approximate Full Adder is considered important for approximate computing to bring out improvements in the efficiency of circuit design. Adders are constituted as the fundamental blocks of arithmetic circuits and are considered important for computation devices. Arithmetic circuits are based on Carbon Nanotube Field Effect Transistor (CNFET)technology and broadly used in image processing, digital signal processing applications. The Carbon nanotube Field Effect transistor is one of the significant areas of research going and adaptable for scaling. It overcome the challenges such as high leakage current, hot effect on electrons, Drain-Induced Barrier Lowering (DIBL), impacts on a short channel effect, etc. They are having of P-type and N-type CNFET's of equal sizes and provide same drive currents, that is essential for reducing the transistor sizes in the complex circuit designs. To evaluate the efficiency between transistor level and application-level simulations HSPICE and MATLAB software are carried out. The results that obtain from HSPICE software with the full adders/multipliers/approximate adders are carried out in applications of image processing.*

Index terms: *Approximate Full Adders, CNFET Energy efficiency, PSNR, SSIM, and Image processing applications*

1. INTRODUCTION

The human eye has a limited vision perception for image and video quality, and it enables circuits to have approximate results rather than accurate. This leads us toward approximate or inexact computation as a recent paradigm in the nano-scale technologies to deal with the problem of power consumption in electronic systems, mostly for image processing applications. The approximation concept is dominating in the field of digital signal processing and multimedia applications as it allows the reduction of area and power significantly with some loss of accuracy. Little inaccuracy does not affect the visual quality as it seems unnoticeable in the perception of a human eye. As an advantage, this technique is to reduce the device utilization for such applications, which will eventually lead to a reduction in terms of power as well as transmission speed. Approximate computing is a well-established paradigm for designing error-tolerant applications such as image & digital signal Processing, including video & sound processing, Internet of Things (IOT) devices, fault-tolerant environments, computer vision, machine learning and sensor networks. Approximate computing aims to reduce the power consumption and design complexity of digital systems with the cost of a tolerable error. the proposed full adders have simple designs and are energy efficient. Approximate computing gives results which are less accurate but with acceptable quality by providing the stringent error requirement.

2. APPROXIMATE FULL ADDER

The Approximate full adder takes place to acquire a quick response in the circuit in the reduction of the delay in the circuitry. The optimization of the design is efficient and the input signal can provide an output with corresponding to the sub-modules of the structural design The FA is the base of most arithmetic operations, such as subtraction, multiplication and division, and, as such, is the main cell of the Arithmetic Logic Unit (ALU) of computing systems. While the functioning of an adding cell is not very complicated, taking into account the frequency of its use, the electrical behavior of FAs becomes critical for the performance of the system. These circuits consist of three inputs, the two bits from the operands (A and B) and a carry-in (Cin), and two outputs

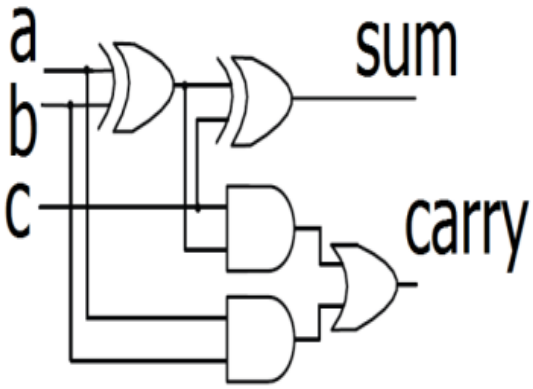

FIGURE 1. bit full adder Convectional diagram

TABLE 1. Truth Table for 1-bit Full Adder

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

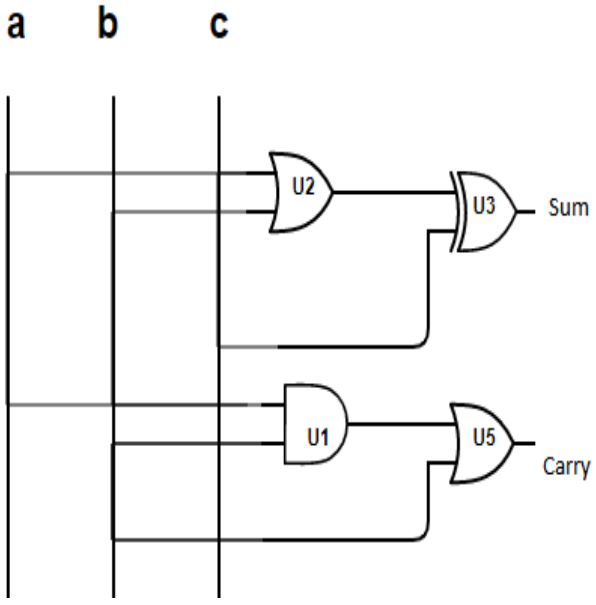

FIGURE 2. Approximate Full adder

3. CNFET

Moore's law states that the number of transistors on integrated circuits (ICs) doubles almost every two years. To sustain this law, the feature size of metal oxide semiconductor field effect transistors (MOSFETs) is aggressively scaled down. Since 2006, the length of the gate of MOSFETs entered deep sub-micron or nano-region at 65nm. But scaling down of the feature size of MOSFETs cannot further help Moore's law to be continued. In fact, MOSFETs at feature sizes below than 65-nm encounter some new challenges such as increase of current leakage, short channel effects, variation in process parameters, reduced gate control, increasing leakage power dissipation, extremely high-power density and so on. To tackle problems of bulk silicon transistors at nanoscale era, some new

technologies such as quantum-dot cellular automata (QCA), single-electron transistor (SET) and carbon nanotube field effect transistor (CNFET) have been emerged. Since emerging of these nanoscale technologies circuit designers have been attracted to conduct their research based on these technologies to overcome problems of nanoscale silicon. Among new technologies, CNFET is one of the most promising successors to the silicon-based technology in the time to come. Carbon Nanotube Field Effect Transistor CNT is a sheet of graphite rolled into a tube. It is discovered by Iijima in 1991. CNT's have widely attracted attention of researchers in different areas such as bio-nano sensors, chemical sensors, transistors, inverters and so forth. In fact, CNFET's have some potential advantages with respect to MOSFETs. A CNT can behave as either conductor or semiconductor, depending on the arrangement angle of carbon atoms along the tube. They consume less power and take advantage of high speed due to their low off-current and near ballistic transport, respectively. Similar to MOSFETs, CNFETs have also two kinds of transistors, p-type and n-type; they have equal mobility with the same transistor geometry that it makes easy transistor sizing of complex digital circuits. Moreover, the current-voltage (I–V) characteristic of a CNFET device is similar to I –V characteristics of MOSFET device. The conductivity of CNT is up 80 times higher than the copper and the mobility charge of electrons and holes values is greater than 100.103 cm2 /Vs compared to 1,5103 cm2 /Vs for amorphous silicon used in the electronics industry. The current density greater than 109. This the three parameters offer CNT good proprieties. Finally, there is a remarkable advantage that makes CNFET to have more advantages against other technologies

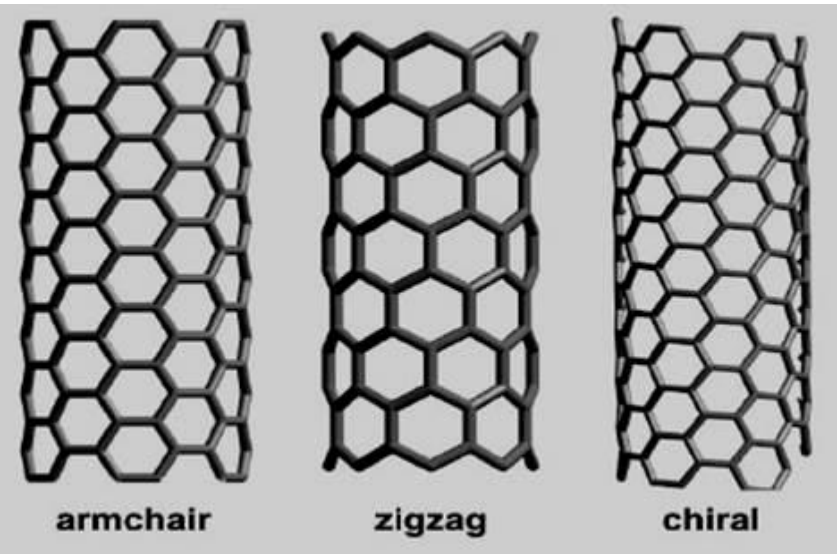

FIGURE 2. Carbon nanotube (CNT) models.

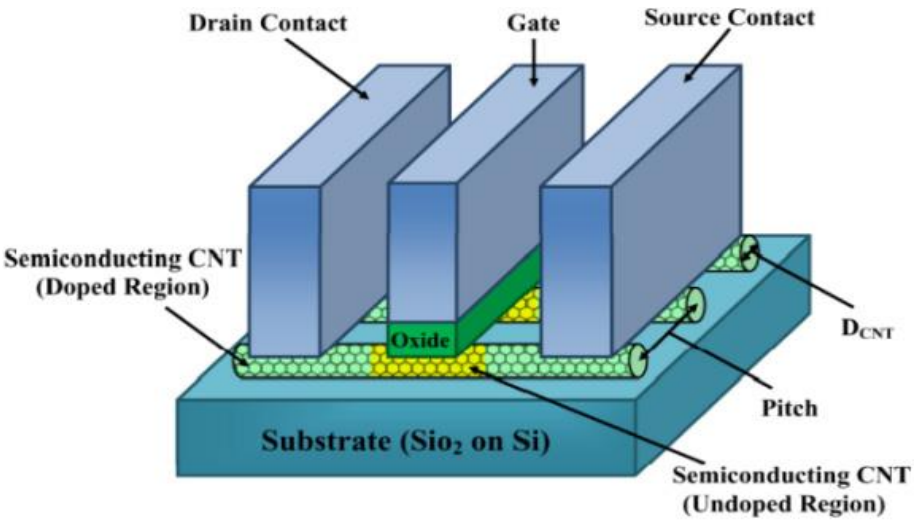

FIGURE 3. CNT transistor

4. CONCLUSION

This paper has presented a literature reviews of Approximate full adders and Carbon nano tube field effect transistor. A Full adder using CNTFETs is a type of logic gate that can be used for image processing applications. This type of logic gate is able to add two binary numbers together, and to produce a sum and a carry bit. The CNTFETs are an attractive choice for this type of application due to their low power consumption, low noise, and high speed. In general, the approximate full adder using CNTFETs can operate at speeds up to 10 times faster than a traditional logic gate, and is a preferred choice for high-speed applications. Additionally, it is capable of working with both positive and negative logic levels, making it a versatile logic gate. Some of the advantages of the approximate full adder using CNTFETs include its low power consumption, high speed, and small size. It's speed and versatility make it an ideal choice for image processing applications.

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