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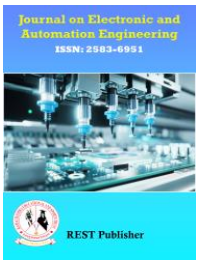

Design and Implementation of Low Power Decoder Using GDI in 90nm Technique

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Abstract: *This paper proposes an innovative approach to address the increasing demand for high-performance, energy-efficient electronic devices. Nowadays, there is a greater demand for integrated circuits that provide top-notch performance, use less power, and remain cost-effective. Our project's aim is to create and implement a low power decoder, which is an important part of modern integrated circuits. Our main goal is to enhance the decoder's design to decrease power usage while maintaining top-notch performance and scalability. To achieve this objective, we explore various VLSI design styles, including CMOS, Transmission Gate Logic (TGL), Pass-transistor Dual-Value Logic (PDVL), and Gate Diffusion Input (GDI). Each of these methodologies present unique advantages in terms of power efficiency, speed, and area utilization. Here the proposed GDI based logic decoder significantly decreases the transistor's count that results in low power consumption. The spread of Cadence (Virtuoso) simulation at 90nm is used for implementing this proposed GDI decoder with different various supply voltages, which shows reduction in power dissipation as compared to typical CMOS and existing mixed logic design*

Index Terms: *This index includes such diverse concepts as Low power decoder, VLSI design styles, Gate Diffusion Input [GDI], Power efficiency.*

1. INTRODUCTION

The main challenge in today's technology world is power consumption.[1] Low power designs play a vital role in all electronics domains such as Integrated Circuits (ICs), System on Chip (SOCs), DSPs, Phase Locked Loop, and Very Large-scale Integration (VLSI) [2]and many other domains.[3] So, there is a great need for applications that use less power and have a smaller area. Static CMOS network consists of one pull-up and one pull-down network, and it gives good output driving capabilities together. There are different CMOS technologies to design any circuit like PTL, TGL etc. Fig.1. shows a CMOS inverter CMOS [4] (Complementary metal-oxide-semiconductor) circuits are used in most logic gates in integrated circuits.

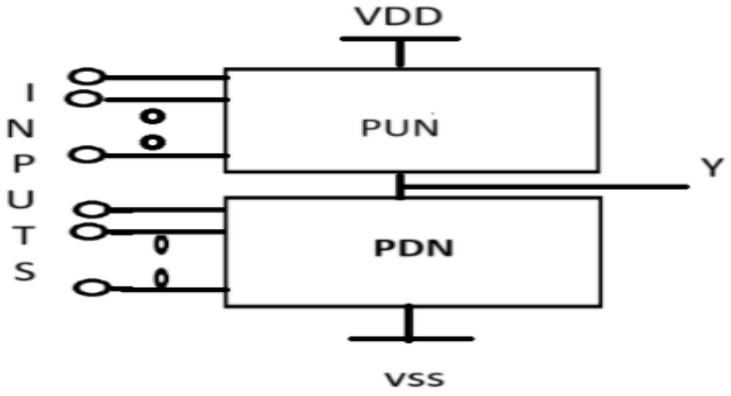

FIGURE 1. CMOS logic gate

They are mainly used because they have almost no static power loss for transistors over 1 µm in length. All designs built with static CMOS consist of two networks: the PUN [Pull Up Network] network and the PDN [Pull Down Network] network. Static CMOS is known for its high current-driving performance and low noise margins. When static CMOS held in a stable state; It uses very little power. CMOS circuits have a major drawback: they can only receive inputs through the transistor gate terminals. This limitation can result in less design flexibility and constraints in cell-based logic design and synthesis. The basic CMOS Inverter is shown in fig 2:

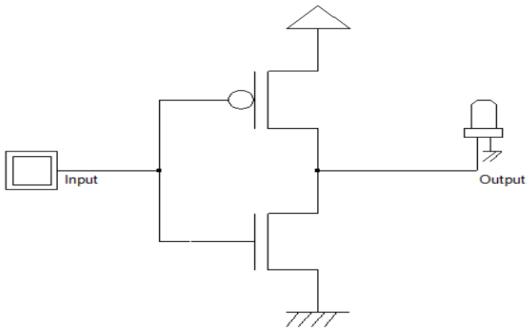

FIGURE 2. Basic CMOS Inverter

CMOS [5] circuits have a major drawback: they can only receive inputs through the transistor gate terminals. This limitation can result in less design flexibility and constraints in cell-based logic design and synthesis. To overcome from this, [6-7] Pass Transistor Logic (PTL) was introduced in the 1990s as an alternative to CMOS logic. PTL offers improvements in speed, power, and area compared to CMOS logic. The main difference in pass transistor circuit design is that inputs are connected to either the gate or source/drain diffusion terminals of the transistors. The figure 3 shows simple PTL circuit:

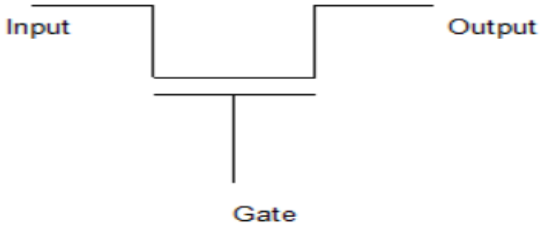

FIGURE 3. Basic PTL circuit

There are two ways to implement pass transistor circuits. The first method uses individual pMOS or nMOS transistors, [8] while the second method uses a parallel combination of pMOS and nMOS transistors called a transmission gate. The figure 4 shows simple TGL circuit:

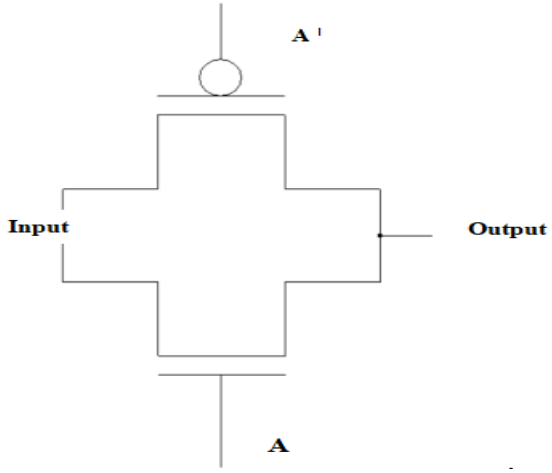

FIGURE 4. Basic TGL circuit

Another advantage of this technique is to reduce the Transistor count by eliminating the redundant logic structures present in conventional static CMOS circuits. The pass transistor reduces the circuits delay; having fewer components reduces the circuit's size and power consumption, but it faces various threshold issues when connected in series. A new approach has been developed by combining static CMOS with pass transistor logic, known as mixed-logic methodology. This method empowers designers to create circuits with enhanced performance. It offers lower power consumption and minimal delay compared to traditional CMOS, making it a reliable technique. The high-performance design is achieved through PTL cell selection and synthesis technique. Decoders, which are a fundamental component of digital circuits, have a wide variety of applications such as address decoding in memory arrays, data demultiplexing, in seven-segment displays, and microchip/microcontroller-based frameworks etc. Address decoders play an important role in SRAM memory block as the power dissipation and access time of SRAM block are largely dependent on design of decoder [12]. This paper presents new technique to design of low power decoder using GDI logic. The GDI strategy is a good choice for designing low-power circuits because it requires fewer transistors than CMOS transistor logic. To enhance logic level swing and reduce static power, a small cell library is used. The rapid growth of portable digital applications has led to a need for faster speed, smaller size, and lower power consumption. This has prompted many analysis efforts [12-14]. Over the past two decades, there have been numerous techniques developed to improve the performance of logic circuits based on traditional CMOS technology [15]. Further, in this paper: Brief explanation about Decoder and its circuit designing by using normal CMOS logic and mixed logic in section II. The proposed decoder technique is explained in section III. Relative simulation results and performance analysis among different designs is discussed in section IV. finally, section V talks about the conclusion

2. EXISTING SYSTEMS

A binary decoder is a multi-input, multi-output combinational circuit that converts a binary code of n input lines into a one out of 2n output code. These are used when there is need to activate exactly one of 2n output based on an n-bit input value. The basic block diagram of Decoder is shown in figure 5:

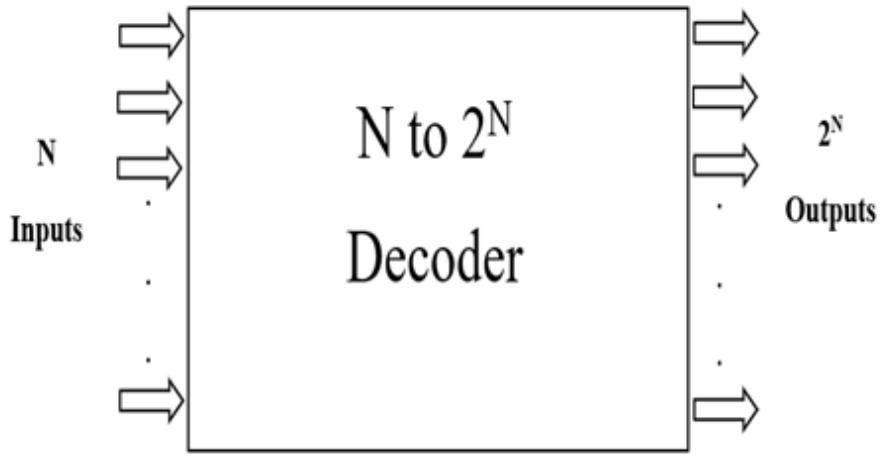

FIGURE 5. Block Diagram of Decoder

2-4 Decoder using conventional CMOS logic

A 2-4 decoder has four outputs labeled D0 to D3, and it takes two inputs A and B. Depending on the input combination, only one output is set to one at a time, while the rest are set to zero. On the other hand, a 2-4 inverting decoder also has four outputs labeled I0 to I3. Depending on the input combination, one output is set to zero while the remaining outputs are set to one. Table 1 shows the truth table for the 2-4 non-inverting decoder, while Table 2 shows the truth table for the 2-4 inverting decoder.

TABLE 1. 2-4 non-inverting decoder truth table

A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

TABLE 2. 2-4 inverting decoder truth table

A	B	I_0	I_1	I_2	I_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	0
1	1	1	1	1	0

Static CMOS circuits are commonly used in conventional decoders. However, direct implementation of AND gates in static CMOS circuits is not possible. Because of issues like more transistor count, high power consumption, more area usage and complex design. To overcome this limitation, universal gates and inverters are employed instead. This approach not only reduces the number of transistors required but also minimizes power consumption and delay. Another reason is NAND/NOR gates in conventional CMOS logic are designed with 4 transistors each, while AND/OR gates require 6 transistors. This is why NAND/NOR gates are preferred over AND/OR gates for efficient logic function implementation in CMOS logic design. A 2-4 non-inverting decoder requires four NOR logic and two inverter logic as depicted in Fig. 6

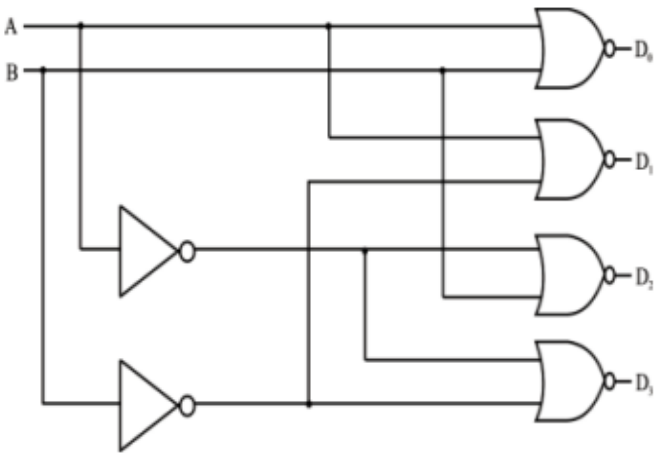

FIGURE 6. 2 to 4 Decoder using NOR Gates

On the other hand, a 2-4 inverting decoder is implemented with four Nand logic and two inverter logic as depicted in Fig. 7:

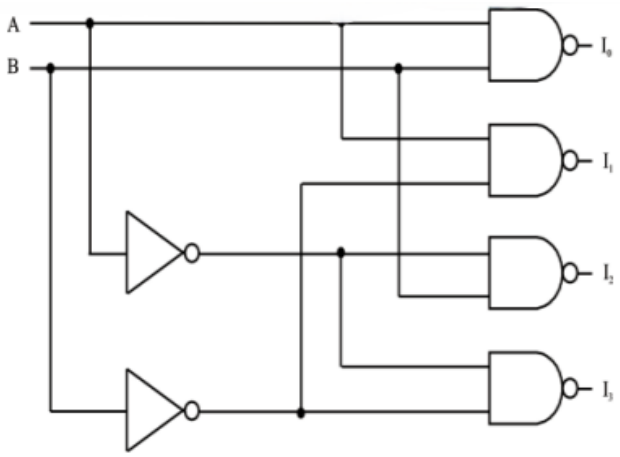

FIGURE 7. 2 to 4 Decoder using NAND Gates

There are still Drawbacks in Static CMOS such as high-power consumption, transistors required up to 20.so we use another methodology called Mixed logic Design.

2-4 Decoder Using Mixed Logic Design

Mixed logic [9] design comprises of transmission gate logic (TGL), conventional CMOS logic and dual value logic (DVL). There are two different circuit styles for implementation of pass transistor logic circuits. First one is Complementary Pass-transistor Logic (CPL) which uses only nMOS pass transistors. Second one uses both pMOs and nMOS pass transistors like Dual Value Logic (DVL) and Double Pass transistor logic (DPL) [6]. DVL is preferred over DPL in mixed logic decoder design due to benefits like lower transistor count and full swing capability. In TGL/DVL 2-input AND/OR are used because AND/OR gates require only 3 transistors when complementary inputs are available. Decoder circuits have a high fanout and multiple gates use only a few inverters. This is why using TGL/DVL gates can lower the transistor count compared to regular CMOS design. The 2-input AND/OR gates using DVL are shown in Fig. 8(a) and 8(b), respectively. The 2-input AND/OR gates using DVL are shown in Fig. 8(c) and 8(d), respectively

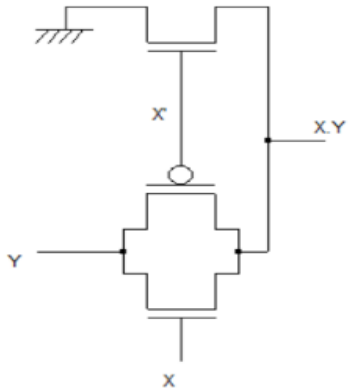

FIGURE 8(A). Transmission Logic AND gate

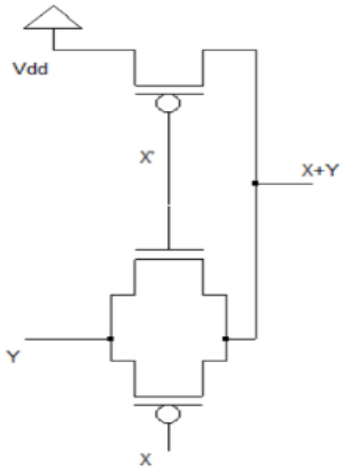

FIGURE 8(B). Transmission Logic OR gate

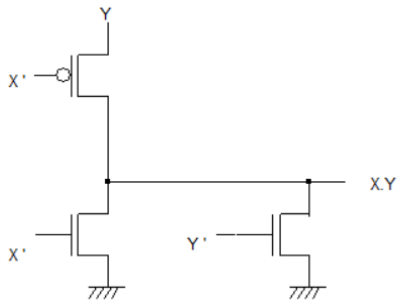

FIGURE 8(c). Dual Value Logic AND gate

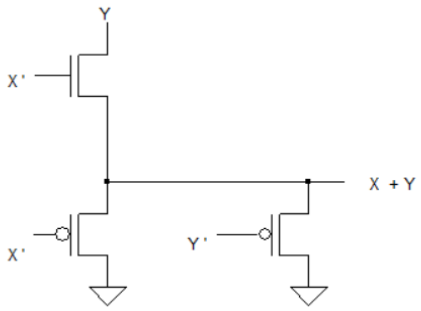

FIGURE 8 (d). Dual Value Logic OR gate

With the help of transmission gate logic and dual value logic AND & OR gates can be easily implemented [8], therefore it is used in decoders. The creation of a mixed logic 2-4 decoder necessitates the utilization of two inverters and four TGL or DVL AND /OR gates, totaling 16 transistors. However, by choosing both TGL and DVL AND gates in the design and carefully selecting control and propagate signals, it is possible to remove one of the inverters, leading to a 14-transistor decoder configuration. To implement a non-inverting decoder, you need to use two inputs, A and B. The outputs D0 and D2 are created using DVL gates [6], with signal A acting as the propagating signal. The outputs D1 and D3 are created using TGL gates, as shown in Figure 9(a). On the other hand, for an inverting decoder, the outputs I0 and I2 are created using TGL gates, and the outputs I1 and I3 are created using DVL gates, as shown in Figure 9(b).

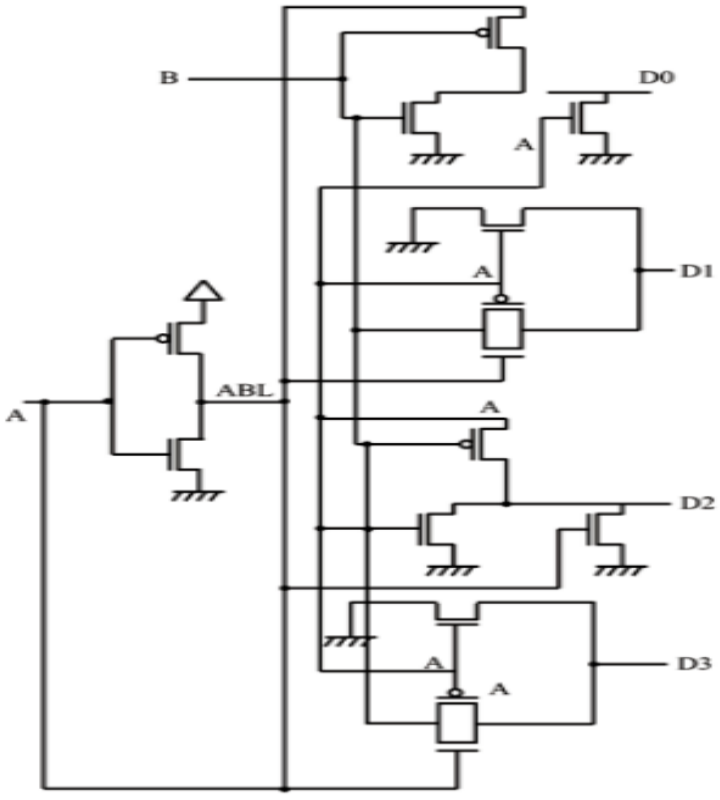

FIGURE 9(a). 2–4 decoders non-inverting decoder

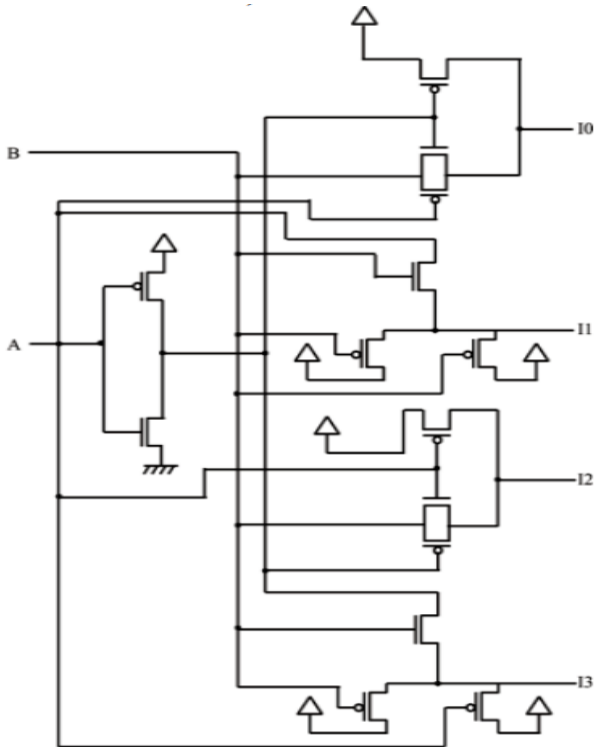

FIGURE 9(b). 2–4 decoders inverting decoder

3. PROPOSED SYSTEMS

This paper analyses a new low power design technique that allows solving most of the problems mentioned in above (as compared to CMOS and existing PTL techniques) digital design circuit techniques i.e. Gate Diffusion Input technique (GDI). The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low power circuits, using reduced number of transistors, while improving logic level swing and static power characteristics.

4. GATE DIFFUSION INPUT (GDI) TECHNIQUE

The GDI method which is first proposed by A. Morgenstern, A. Fish, and I. A. Wagner in 2001 [11]. The basic cell of GDI is shown in fig 10:

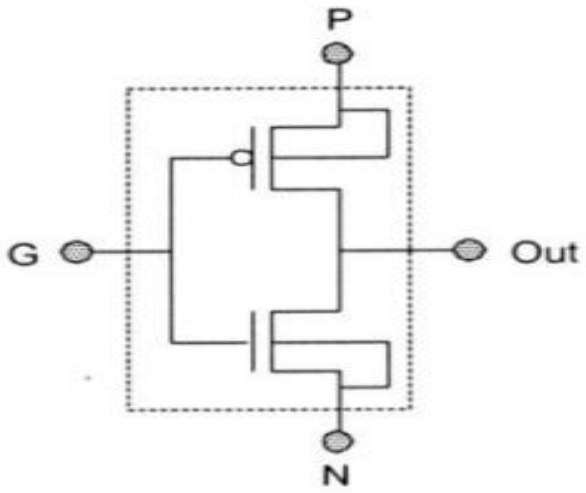

FIGURE 10. GDI Basic Cell

At first glance, the basic cell reminds the standard CMOS inverter, but there are some important differences:

- The GDI cell contains three inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS).
- Bulks of both nMOS and pMOS are connected to N or P (respectively), so there are differences with a CMOS inverter.

GDI cell very suitable for implementation of any logic function that was written by Shannon expansion. Shannon expansion is a technique used in digital circuit design and Boolean algebra to simplify logic expressions. It's named after Claude Shannon, a pioneer in the field of digital circuit design and information theory, by combining Shannon expansion techniques [18] with GDI cells, designers can achieve efficient and low-power implementations of combinatorial circuits in VLSI design.

Table 1 shows the input logic combinations to perform various functions using GDI technique. Comparison of CMOS and GDI is made in Table I in terms of transistor count.

TABLE 3. Various Logic Functions Using Gdi Cell and Their Input Combinations

Basic functions using GDI Cell					No. of transistors	
G	P	N	FUNC	OUTPUT	GDI	CMOS
A	B	1	OR	A+B	2	6
A	0	B	AND	A.B	2	6
A	B	C	MUX	$\bar{A}.B + A.C$	2	12
A	B	$\bar{A}$	XOR	$\bar{A}.B + A.\bar{B}$	4	16
A	1	0	INV	$\bar{A}$	2	2

Analysis of GDI technique

In the updated mixed logic design, the transmission gate component of the decoder, which was previously used in the mixed logic decoder, has been replaced with the full swing GDI technique. In this we implement the GDI logic technique using DVL, AND and OR gates. This means that a decoder can now be created by combining GDI and DVL with the conventional CMOS inverter. Figure 11(a), (b), (c), and (d) display the GDI-based AND/OR gates [16]-[17] and the DVL-based two-input AND/OR gates.

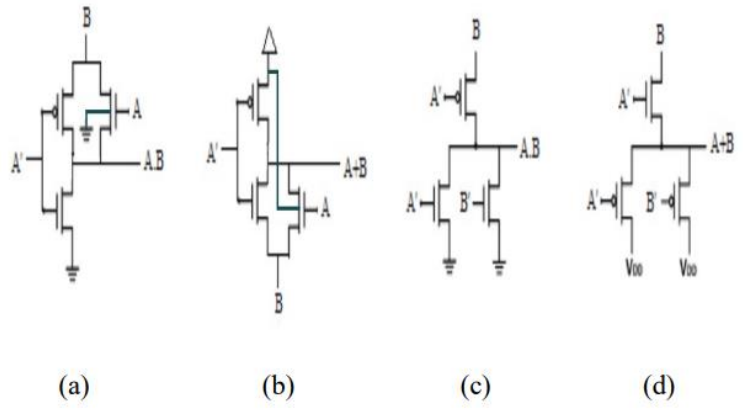

FIGURE 11. AND/OR gates (a) GDI based AND Logic. (b) GDI based OR logic. (c) DVL based AND logic. (d) DVL based OR logic.

In Figure 11, we can see that there are two gate inputs labeled A and B. In GDI based AND/OR gates, input A controls the gate terminals of all three transistors. However, in DVL based AND/OR gates, input A is connected to the gate terminals of two transistors, while input B controls the gate terminal of one transistor. Input B also acts as a propagating signal.

2-4 Decoder using GDI logic

To design a 2-4 decoder using static CMOS requires up to 20 transistors, and it also consumes more power. To overcome this, mixed logic design was introduced. Through mixed logic design, it requires 14 transistors but has decent power consumption compared to CMOS. So, we try to design a 2-4 decoder using a new technique called GDI. The schematic of the 2-4 decoder using GDI is shown in Fig 12. It uses three different methodologies for every output. For D0, it uses the GDI technique; for D1, it employs the TGL technique; for D2, it utilizes the DVL technique, and for D3, it again utilizes the GDI technique. So, the total transistor count is 12. In this, we have two inputs, A and B. The input A is attached to a CMOS inverter. So finally, there is a decreased transistor count in GDI decoder compared to 20 transistors in CMOS and 14 transistors in mixed logic designs. There is a reduction in power dissipation of the GDI circuits compared to CMOS and Mixed logic designs

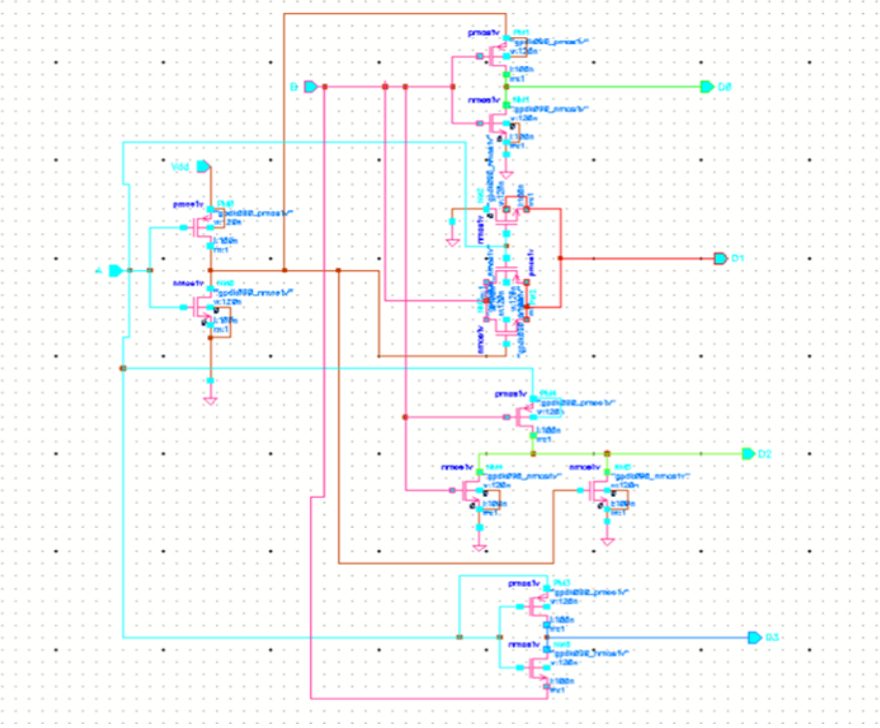

FIGURE 12. 12 2-4 decoder design using GDI

5. RESULTS & DISCUSSIONS

Results: A range of Cadence Virtuoso based simulations is performed for comparing GDI based 2-4 decoder with existing mixed logic and conventional CMOS based decoders. All circuits are designed in 90nm technology to get reliable outputs. All designs are analyzed at voltage (0.8V, 1.2 V). Input/output waveforms of non-inverting decoders using the proposed method are depicted in Fig. 13.

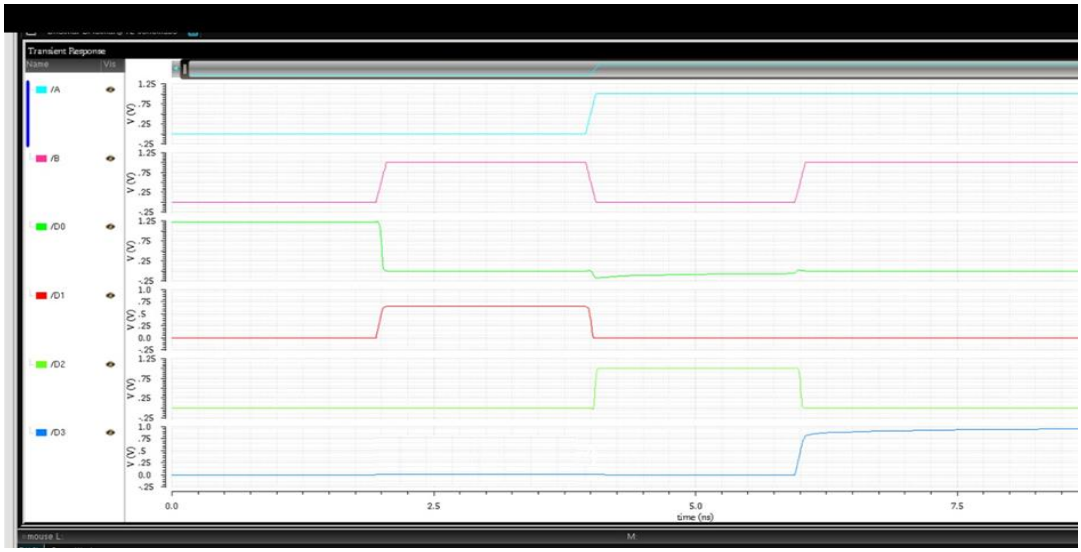

FIGURE 13. I/O waveforms of proposed 2-4 decoder

Performance Analysis

The parameters taken for the analysis are Power dissipation. Various performance analyses are given in Table 4 for power dissipation. Each proposed design technique is compared with conventional CMOS logic technique.

TABLE 4. Power Dissipation For 2-4 Decoders

Decoders	Power(µW)			
	CMOS		GDI	
	0.8V	1.2V	0.8V	1.2V
2-4 Decoder	0.365	0.402	0.142	0.219

6. CONCLUSION

This paper proposed a GDI technique and implemented a 2-4 decoder. The analysis concludes that proposed 2-4 decoder consumes less power compared to existing mixed logic and conventional CMOS based 2-4 decoders.

Acknowledgement: We would like to thank all the authors in the references for providing great knowledge and helpful advice whenever required.

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