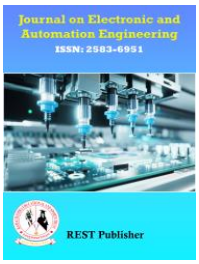
Journal on Electronic and Automation Engineering

Vol: 4(2), June 2025

REST Publisher; ISSN: 2583-6951 (Online)

Website: https://restpublisher.com/journals/jeae/

DOI: https://doi.org/10.46632/jeae/4/2/22



Comparative Analysis of Ternary Half Adder Using CNTFET

***P. Anusha, U. Anitha, M. Chenna kesava Reddy, S. Musthakim, S.V. Chanikya Rao, E. Kalyana Pallavi**

Annamacharya Institute of Technology and Sciences, Kadapa, Andhra Pradesh, India.

**Corresponding author Email: anulakshmi1728@gmail.com*

Abstract: *Ternary logic, a form of multi-valued logic (MVL), presents a promising alternative to traditional binary logic by enhancing computation efficiency, circuit density, and power savings. This study conducts a comparative analysis of two ternary half adder (THA) designs: a multiplexer-based approach and a decoder-based approach, implemented using carbon nanotube field-effect transistors (CNTFETs). The multiplexer-based THA utilizes 90 transistors, while the decoder-based design employs 74 transistors. Both designs were simulated using HSPICE with Stanford's 32nm CNTFET technology at a supply voltage of 0.9V. The results highlight the trade-offs between transistor count, power consumption, and operational speed, providing insights into the efficiency and suitability of each design for low-power, high-performance ternary arithmetic circuits. The comparative evaluation underscores the advantages and limitations of multiplexer and decoder-based architectures in the context of nanoscale computing platforms.*

1. INTRODUCTION

The electronics industry is increasingly focused on the miniaturization of integrated circuits to achieve higher performance, reduced power consumption, and smaller physical footprints [1–3]. In alignment with Moore's Law, the semiconductor industry continuously works to shrink the dimensions of metal-oxide-semiconductor field-effect transistors (MOSFETs), effectively doubling the number of transistors on a chip with each technology node [4]. However, as technology advances into the sub-32nm regime, MOSFETs encounter several critical challenges [5]. These include short-channel effects (SCEs), reduced gate control, higher power density, increased device variability, and significant subthreshold leakage currents [6]. These factors collectively degrade device performance and limit the feasibility of MOSFETs in energy-efficient applications [6].To address these limitations, alternative transistor technologies are being explored. Carbon nanotube field-effect transistors (CNTFETs) have gained substantial interest due to their excellent electrical properties and superior energy efficiency. Similar in operation to MOSFETs, CNTFETs are well-suited for nanoscale circuit design, making them a strong candidate for next-generation electronics [7,8]. Conventional digital systems operate using binary logic, where inputs and outputs are restricted to two discrete states—'0' (0V) and '1' (VDD). Binary logic gates are foundational elements in electronic devices such as calculators and computers, forming the basis of digital computing [9]. Despite their widespread use, binary logic circuits suffer from scalability issues. As complexity increases, the number of required interconnections grows, leading to larger chip sizes and greater energy and power demands [10–11]. Multiple-valued logic (MVL) presents a promising solution by extending logic beyond two states. MVL gates, capable of handling more than two logic levels, offer several advantages such as improved data compression and a significant reduction in interconnect complexity for complex circuits [12]. While the theoretical optimal base for MVL is the mathematical constant *e* (approximately 2.718), hardware constraints necessitate the use of integer bases. Among these, ternary logic (base-3) has emerged as the most practical and efficient choice [13,14]. Ternary logic systems have demonstrated the potential to reduce chip area by up to 70% and power consumption by up to 50% when compared to traditional binary systems [15]. Arithmetic circuits, especially adders and multipliers, are critical components in digital architectures. These components are extensively used in very-large-scale integration (VLSI) applications, including digital signal processing (DSP), microprocessors, and image or video processing systems [6,8,16,17]. Incorporating ternary logic with CNTFET technology in these systems offers a powerful approach for achieving high-performance, compact, and energy-efficient designs. A carbon nanotube field-

effect transistor with many channels (multi-CNTFET) is depicted in the image below. The device is positioned on a substrate in the front view (Fig. 1(a)), which is covered with a bulk dielectric layer that acts as an insulating base. The gate electrode is electrically isolated from the channel region by a gate dielectric layer placed above it. The source and drain terminals, which are positioned on either side of the gate, have their current flow modulated by the centrally situated gate electrode. A voltage applied to the gate allows electron transport across the channel's doped carbon nanotubes (CNTs), which link the source and drain. The device's layout is shown in the top view (Fig. 1(b)), which also highlights important structural factors. The distance across which the CNTs extend is indicated by the channel length (Lch), and the gate is symmetrically positioned between the source and drain terminals. To improve device performance and reduce short-channel effects, areas known as Lightly Doped Drain (Ldd) and Lightly Doped Source (Lss) are added. The pitch between neighboring CNTs and the gate width(Wgate) are additional crucial variables that have a big impact on the device's integration density and current carrying capacity. High-speed operation, enhanced scalability, and lower power consumption are just a few benefits that this multi-CNTFET arrangement offers for nanoscale electronics. The multi-threshold voltages (Vth) approach is the appropriate method for creating and putting into practice ternary circuits, as mentioned in [18]. One well-known method for creating multi-threshold designs in a MOSFET is body biasing. Delivering biasing to most MOSFETs with different voltages is a challenging and delicate procedure that mostly occurs during the fabrication process [9,19]. Circuits with multiple Vth can be designed and implemented using CNTFETs; the necessary Vth is achieved by considering the proper CNT diameters [4].

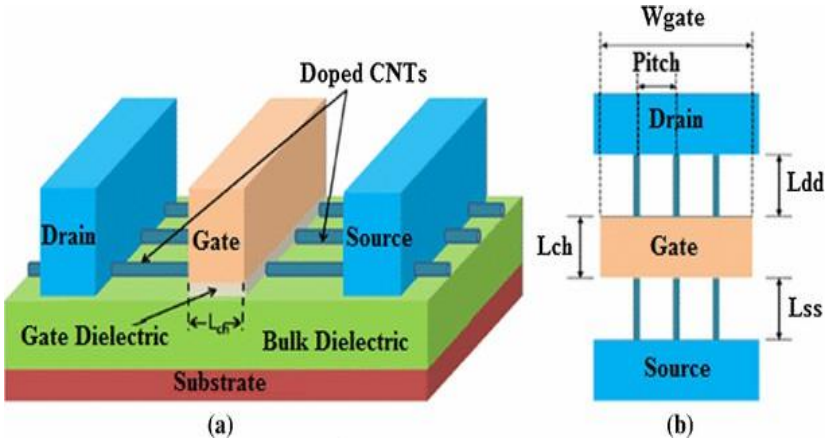


FIGURE 1. A multi-CNTFET [8], (a) Front-view and (b) Top-view

2. PRELIMINARIES

2.1 CNTFET:

Carbon Nanotubes (CNTs) are nanoscale cylindrical structures made of rolled graphene sheets and are classified into two types: single-walled carbon nanotubes (SWCNTs), consisting of a single graphene cylinder, and multi-walled carbon nanotubes (MWCNTs), which comprise two or more concentric cylinders [21,22]. The electronic properties of a SWCNT are determined by its chirality vector, represented by the integer pair (n, m), which defines the arrangement of carbon atoms along the tube.SWCNTs can behave either as conductors or semiconductors depending on the values of *n* and *m*. If the difference *(n – m)* is a multiple of 3 (i.e., *n – m = 3k*, where *k* is a positive integer), the SWCNT exhibits metallic properties and is suitable for use as an interconnect. Conversely, if *(n – m)* is not a multiple of 3, the SWCNT exhibits semiconducting behavior and can be used as the channel material in field-effect transistors (FETs) [21,23]. As shown in Fig. 1, the structure of a multi-CNTFET is illustrated. Similar to CMOSFETs, CNTFETs operate based on a threshold voltage (V_{th}) that controls the gate to switch the device on or off. However, what distinguishes CNTFETs is their ability to tune the threshold voltage through the selection of CNT diameters. This unique characteristic allows the design of multi-threshold voltage (multi-V_{th}) circuits, offering greater flexibility for digital circuit design. The threshold voltage of a CNTFET can be calculated using Equation (1) [24,25].

$$v_{th} \cong \frac{Eg}{2e} = \frac{\sqrt{3}}{3}\frac{av_{\Pi}}{eDC_NT} \cong \frac{0.43}{D_{cNT}} \quad (1)$$

where Vπ≅3.033eV is the π-π band energy of ca rbon in tight bonding model, a=0.249nm is gap between carbon atoms, e is electron- charge, and DCNT is CNT diameter, that is calculated by Eq. (2) [24,25]:

$$DCNT = \frac{a\times\sqrt{n^2+m^2+nm}}{\pi} \sim^{0.783}\sqrt{n^2+m^2+nm}$$

The CNTFET device's gate width, denoted by WGate, is equated by Eq. (3), whereas pitch is gap between the two CNTs and ntube is nanotubes number [24,25].

TABLE 1. The Vth values and ON/OFF conditions of CNTFETs, categorized based on the chiral values employed [5]

$$\text{WGate} = \text{pitch} \times (n_{tube}\text{- } 1) + D_{CNT} \quad (3)$$

CNTFET device	Chiral value (n, m)	Vth	VGS (V) 0	0.45	0.9
P- type	(10,0)	-0.56V	ON	OFF	OFF
	(19,0)	-0.29V	ON	ON	OFF
N- type	(10,0)	0.56V	OFF	OFF	ON
	(19,0)	0.29V	OFF	ON	ON

Table 1 summarizes the threshold voltage (V_{th}) requirements for CNTFETs in their ON and OFF states [5]. For instance, a CNT with chirality (10, 0) exhibits a relatively high threshold voltage of 0.56 V, whereas a CNT with chirality (19, 0) has a lower threshold voltage of 0.29 V, demonstrating the direct influence of chirality on device behaviour. Various types of Carbon Nanotube Field-Effect Transistors (CNTFETs) have been introduced in the literature, each offering unique advantages, limitations, and operational characteristics. One widely studied type is the Schottky-Barrier (SB) CNTFET, which operates through electron tunneling at the metal–semiconductor junction located at the source–channel interface. This type is formed by directly contacting the carbon nanotube (CNT) with metal, creating a Schottky Barrier. However, the presence of this barrier restricts the device's transconductance and on-state current, limiting its performance in high-speed applications. Another variant is the Band-to-Band Tunneling (BTBT) CNTFET, which enables electron flow by allowing tunneling through the energy bandgap of the device. Although this type typically exhibits lower on-state current, it offers excellent cut-off characteristics and is particularly effective for low-power and sub-threshold applications due to its energy efficiency.The MOSFET-like CNTFET is designed to replicate conventional MOSFET behavior while offering enhanced performance. This is achieved by eliminating the Schottky Barrier at the source–channel interface through the formation of heavily doped CNT regions at both the source and drain terminals. As a result, the device achieves higher on-state currents, making it well-suited for high-speed, fast-switching digital applications [4,6,21,26].

TABLE 2. Basic ternary operations [23].

Operations	Expression
OR	$xi+xj=max(xi,xj)$
AND	$xi.xj=min\{xi,xj\}$
NOT	$\bar{x_1} = 2 - x_i$

2.2. Ternary Systems:

In place of the conventional binary system, ternary logic employs three values [23]. In 1840, Thomas Fowler made the initial proposal [27]. Ternary can be described as either unbalanced {0, 1, 2} or balanced {-1, 0, 1}. The imbalanced mode, which is equal to { 0V, VDD/2, V DD } [1,18], is employed in this study.The AND, OR, and NOT operations are described in Table 2 [23]. Universal gates and inverters are the basic building blocks of ternary systems. The equations given in Table 2[23] govern how these gates operate. An inverter is the most commonly used fundamental gate in digital design. Standard, positive, and negative inverters (STI, PTI, and NTI, respectively) are the three types of inverters found in ternary systems. The ternary input is X = {0 -2}, the NTI and PTI are represented by $x_N$and x_P, respectively, and the STI of $\bar{x}$ is indicated by the overline x. Equation 4 provides their related equations [28]. Figure 2 displays the PTI and NTI schematics [5].

$$x_N = \begin{cases} 0, if\ x \neq 0 \\ 2, if\ x = 0 \end{cases} \quad (4a)$$

$$x_P = \begin{cases} 2, if\ x \neq 2 \\ 0, if\ x = 2 \end{cases} \quad (4b)$$

$$\bar{x} = 2 - x \quad (4c)$$

The Eqs. (5a) and (5b) are used to define the NAND (TNAND) and NOR (TNOR) as two-input functions for two

inputs *A* and *B* [23].

$$\text{TNAND} = \overline{min\{A, B\}} \quad (5a)$$

$$\text{TNOR} = \overline{max\{A, B\}} \quad (5b)$$

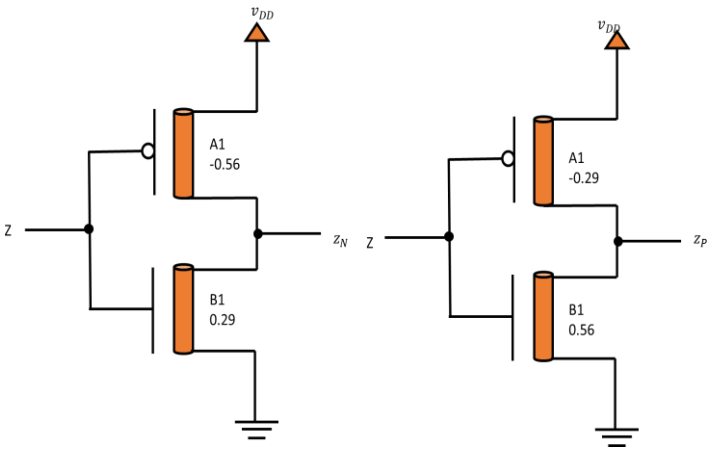


FIGURE 2. Circuit diagrams of the (a) NTI and (b) PTI

Fig.2. shows the circuit diagrams of NTI and PTI. NTI is one of the types of inverters used in ternary logic systems, which operate using three distinct voltage levels instead of the two levels used in binary logic. These ternary values are usually represented as: 0 (Low / GND),1 (Middle / $^{v_{dd}}/_{2}$), 2 (High / v_{dd}). PTI is another type of ternary inverter, just like NTI, but it behaves oppositely in some sense. In a ternary logic system with three voltage levels: 0 → Low (Ground), 1 → Mid-level ($^{v_{dd}}/_{2}$),2 → High (v_{dd}).

3. CNTFET-BASED TERNARY CIRCUITS

Ternary Half – Adder

A Ternary Half Adder (THA) is a two-input, two-output circuit that adds two ternary inputs, A and B, and produces two outputs: sum and carry. The behavior of the THA is defined by its truth table, as shown in Table 3. To implement the THA, Jaber et al. [10] began with Equation (6), which represents the conventional THA formulation commonly used in previous works [15,36], and derived a simplified version presented as Equation (7).

TABLE 3. THA truth table

Input A	B	Output sum	carry
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

Multiplexer Based Ternary Half Adder

A 3:1 multiplexer is a combinational logic circuit that selects one of three input signals I_0, I_1, & I_2 and routes it to a single output B, based on the values of the selection lines**.** A Ternary Multiplexer (TMUX) is a digital circuit used in multi-valued logic systems to select one of three input signals I_0, I_1, or I_2 based on a ternary control signal Z. Unlike traditional binary multiplexers, the control signal in a TMUX can assume three discrete logic levels: 0, 1, or 2. This allows the TMUX to route one of the three inputs to the output B depending on the value of Z. Specifically, when Z = 0, the output B is equal to I_0; when Z = 1, the output is I_1; and when Z = 2, the output is I_2. Such functionality is highly efficient in ternary logic systems, as it reduces the need for multiple binary components and enhances circuit compactness and performance.

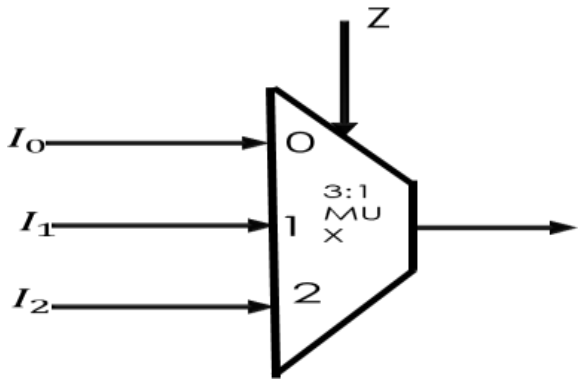


FIGURE 3. Circuit of ternary multiplexer, (a) Symbol

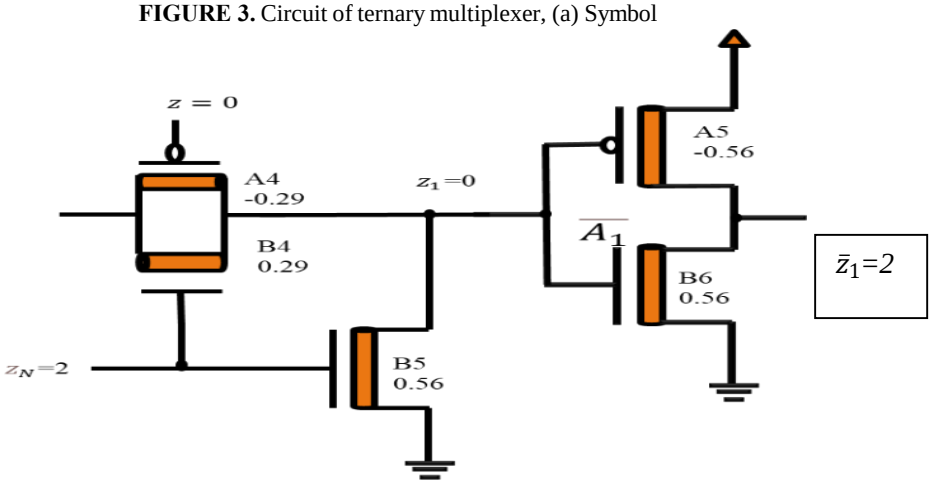


FIGURE 4. Circuit of ternary multiplexer (b) Transistor - level structure [10]

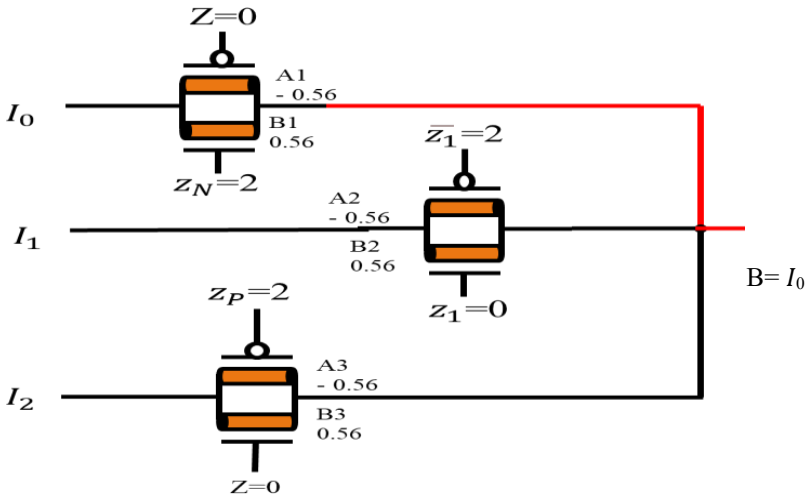


FIGURE 5. Ckt of ternary multiplier, transistor-level structure[10]

Table 4. Selection Table

Z	B
0	I_0
1	I_1
2	I_2

TABLE 5. Truth table of Ternary Multiplexer

z	z_N	z_P	z_1	$\overline{z_1}$
0	2	2	0	2
1	0	2	2	0
2	0	0	0	0

A Ternary Multiplexer (TMUX) routes one of three input signals to the output based on the value of a ternary control signal **Z**, which can take values 0, 1, or 2. TMUXes are essential components in ternary logic design, serving as foundational elements for implementing various ternary functions. They are widely used in the construction of arithmetic circuits such as ternary half adders and full adders by enabling efficient signal selection and logic function realization. TMUX-based designs have been shown to simplify the implementation of ternary systems, making them highly suitable for multi-valued logic architectures. In ternary computing, where each signal represents one of three possible states, TMUXes contribute to improved data handling, reduced circuit complexity, and enhanced processing efficiency. Their usefulness also extends to communication systems, where they enable the simultaneous transmission of multiple data types—such as audio and video—over a single line, increasing overall bandwidth utilization. Figure 4 presents an existing Ternary Half Adder (THA) circuit, verified against its corresponding truth table (Table 3). The design includes three multiplexers: the first, on the left, takes inputs **1, 2, and 0** and selects one based on input **X**; the second, in the center, takes **2, 0, and 1**, also selected by **X**; and the third, on the right, takes inputs **X** and **2**, selected based on input **Y**. The outputs of the first and second MUXes feed into the third MUX, which generates the final output for the sum function of the THA.

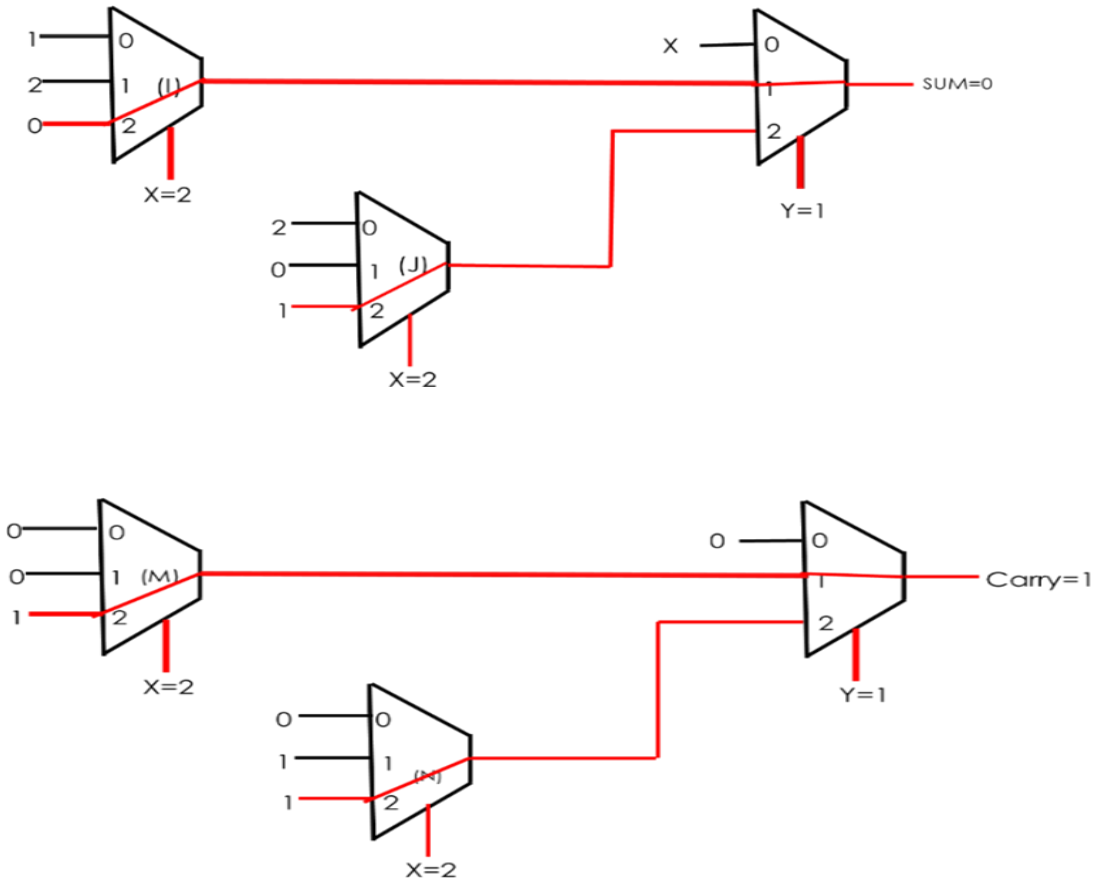


FIGURE 6. Schematic version of Mux- Based THA proposed by Jaber et al. [10]

When the Sum circuit is evaluated with **X = 2** and **Y = 1**, the first MUX (on the left) selects the input labeled "2" corresponding to **X = 2**, producing an output of **0**. Similarly, the second MUX (center) also selects its "2" input due to **X = 2**, resulting in an output of **1**. The third MUX (on the right) makes its selection based on **Y = 1**, thereby choosing the output from the second MUX, which is **1**, and ultimately produces a final output of **0**.

$$\text{Sum} = 2 \cdot (A_0B_2 + A_1B_1 + A_2B_0) + 1 \cdot (A_0B_1 + A_1B_0 + A_2B_2)$$

$$\text{Carry} = 1 \cdot (A_1B_2 + A_2B_1 + A_2B_2) \quad (6)$$

$$\text{Sum} = A \cdot B_0 + (1.A_0 + 2.A_1 + 0.A_2).B_1 + (2.A_0 + 0.A_1 + 1.A_2).B_2$$

$$\text{Carry} = 0.B_0 + (0.A_0 + 0.A_1 + 1.A_2).B_1 + (0.A_0 + 1.A_1 + 1.A_2).B_2 \quad (7)$$

A Ternary Half Adder (THA) can be constructed using six 3:1 Ternary Multiplexer (TMUX) circuits, as represented by Equation (6). Each 3:1 TMUX operates by selecting one of three input signals I_0, I_1, or I_2 based on the value of a selection signal X, and forwarding it to the output Z. The operation of the 3:1 TMUX is defined by Equation (8), as outlined in [10].

$$Z = I_0x_0 + I_1x_1 + I_2x_2 \quad (8a)$$

$$Z = \begin{cases} I_0, if\ x = 0 \\ I_1, if\ x = 1 \\ I_2, if x = 2 \end{cases} \quad (8b)$$

As illustrated in Fig. 3, Jaber et al. [10] introduced a CNTFET-based 3:1 TMUX design that functions without a ternary decoder, utilizing only 15 transistors. Building on this structure, they designed a CNTFET-based Ternary Half Adder (THA), shown in Fig. 4, which consists of 90 transistors. In this implementation, the inputs **A** and **B** are used as selection signals for the TMUX circuits. However, a major drawback of the design is the need to repeatedly generate the selection signals, leading to increased circuit complexity.

Decoder Based Ternary Half Adder

A decoder-based Ternary Half Adder (THA) utilizes ternary decoders to implement the logic required for generating sum and carry outputs from two ternary inputs. In this approach, the inputs A and B are first passed through ternary decoders, which convert the input values into a set of control signals. These signals are then used to drive logic blocks that compute the appropriate sum and carry outputs based on the ternary truth table. This design offers structured logic implementation and simplifies circuit synthesis. However, it typically results in higher transistor count and increased power consumption. In one such design, a total of 74 CNTFETs are used, making it less efficient than transistor-optimized alternatives. Despite its overhead, decoder-based THA designs are useful in applications where modularity and clarity in logic expression are prioritized.

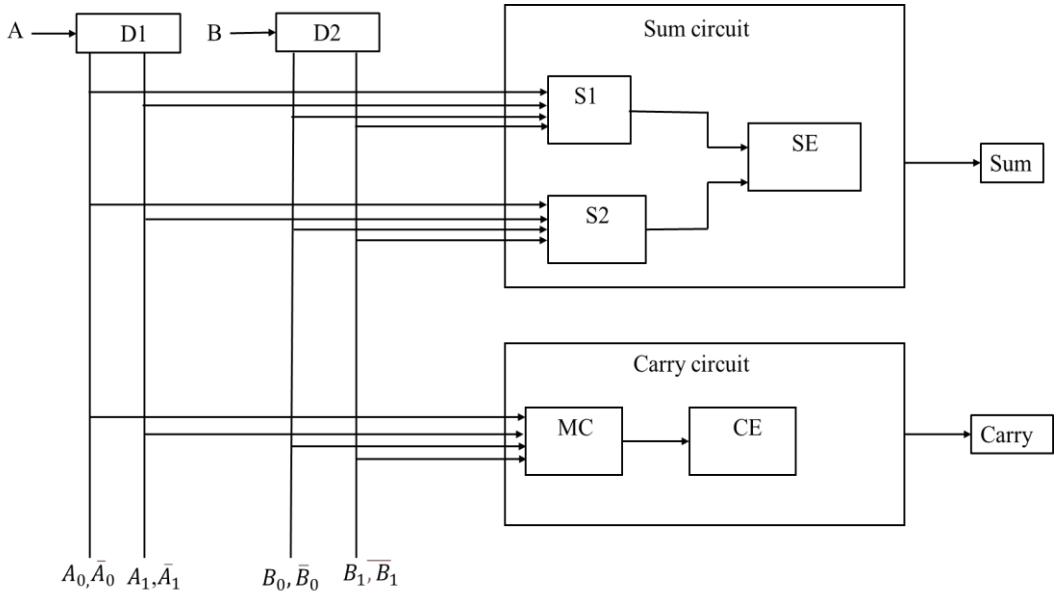


FIGURE 7. Block diagram of ternary half adder [42]

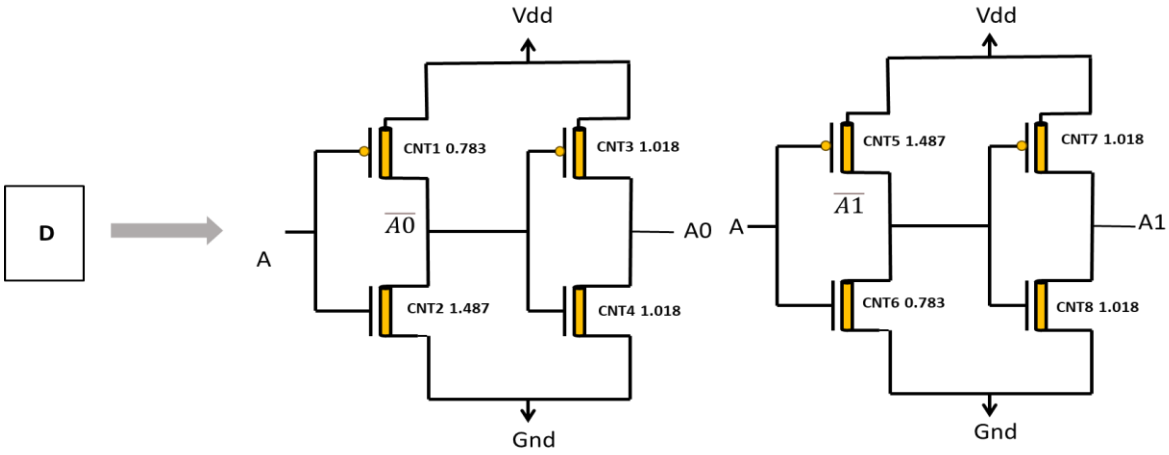
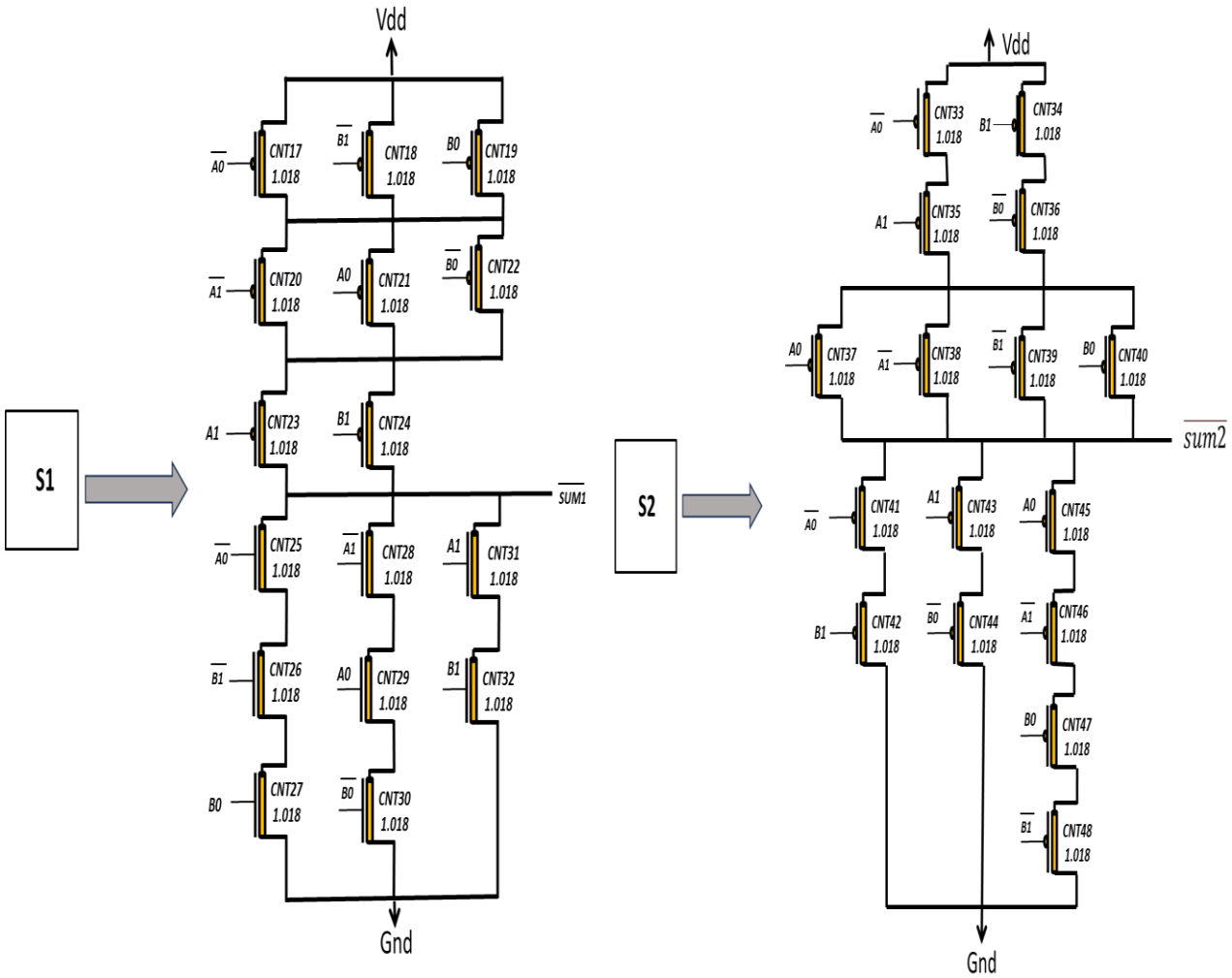


FIGURE 8. Decoder Circuit



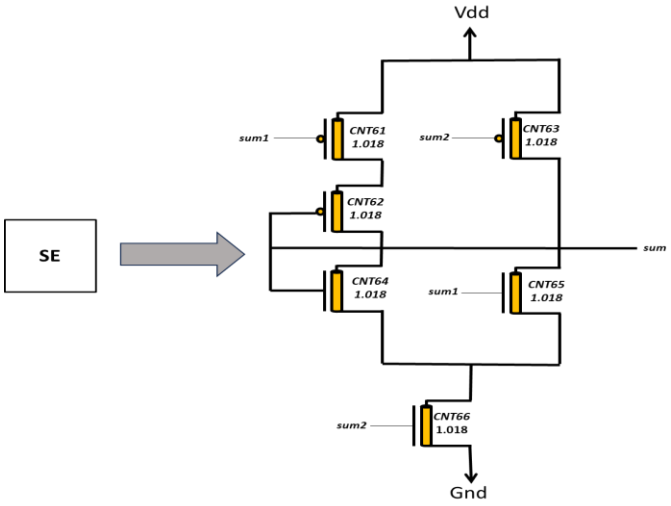


FIGURE 9. Sum Circuit

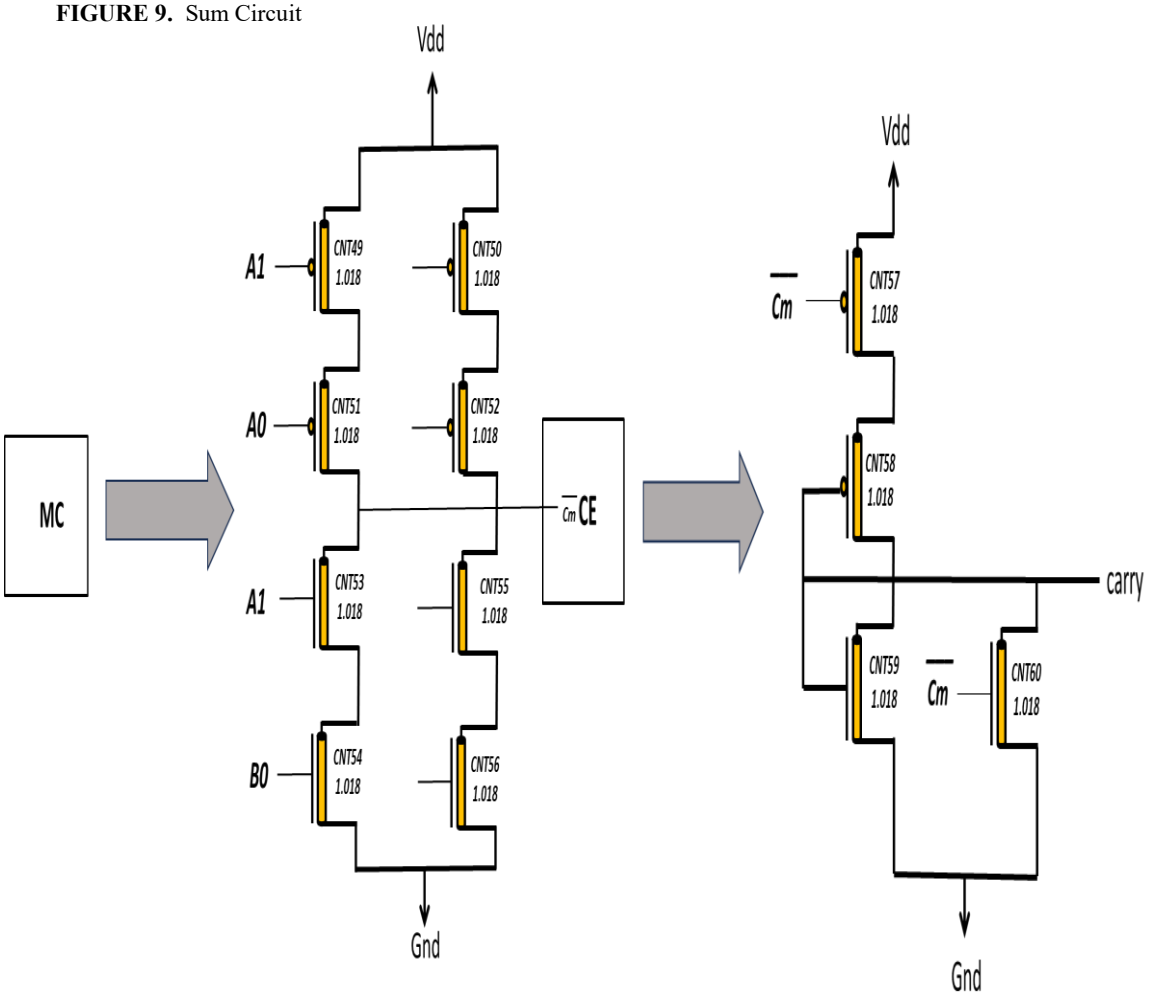


FIGURE 10. Carry generation

The Ternary Half Adder, a key part of ternary logic systems, is depicted in the figures along with its design and operation. The block diagram in Figure 5 shows two input decoders that transform ternary values into signals that resemble binary before sum and carry circuits handle them. A middle carry stage and a carry encoder are used in the carry circuit to determine the carry output, while the sum circuit uses intermediate signals (Sum1 and Sum2) and a sum encoder to compute the ternary sum. The decoder circuit, shown in Figure 6, uses CMOS transistors to transform ternary inputs into two output signals (A0, A1) for additional processing. The sum

circuit is described in full in Figure 7, which displays a logic system based on transistors that can carry out ternary addition. In a similar manner, Figure 8 illustrates the carry generating method, showing how the circuit generates the carry output by evaluating various ternary input circumstances. Because CMOS transistor-based logic is used throughout the design, multi-valued logic computations are more efficient due to lower circuit complexity and power consumption. The decoder-based ternary half adder consists of 74 transistors. The main disadvantages of decoder-based ternary half adders are higher power consumption and slower speeds. Using a decoder to create a ternary half adder results in decoding all ternary input combinations, which increases the size and complexity.

Waveforms

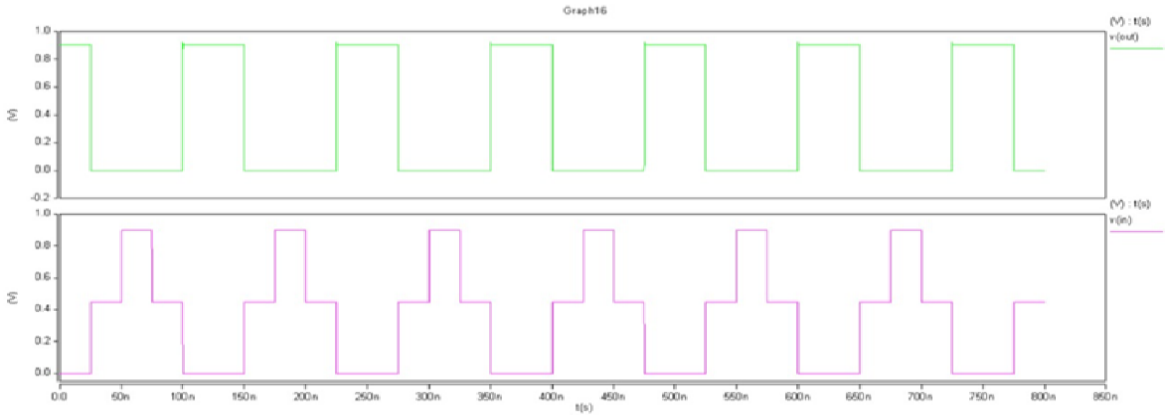


FIGURE 11. Stimulation outputs for NTI

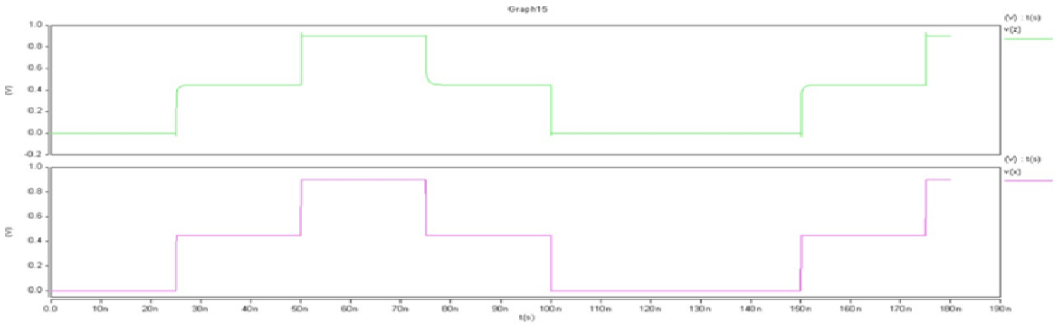


FIGURE 12. Stimulation outputs for PTI

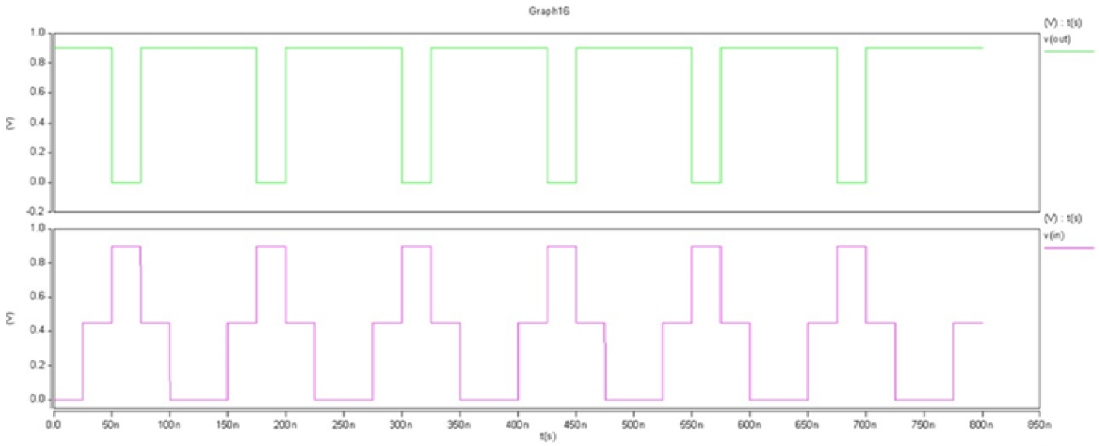


FIGURE 13. Simulation outputs for THA

4. RESULTS AND DISCUSSIONS

TABLE 6. Comparison for Ternary Systems

Ternary Systems	POWER (n W)	DELAY (p s)	PDP (z J)	EDP (q Js)	No. of Transistors
NTI	4.8313	24.941	120.49	3.0051	2
PTI	5.4381	19.707	107.16	2.1119	2
TMUX	4.4162	46.062	203.41	9.3698	15

TABLE 7. Comparison for Ternary Half Adder

Ternary Half- Adder	**POWER (n W)**	**DELAY (p s)**	**PDP (z J)**	**EDP (q Js)**	**No. of Transistors**
Mux- Based	37.952	79.957	3034.5	242.63	90
Decoder-Based	30.728	76.248	2342.9	178.645	74

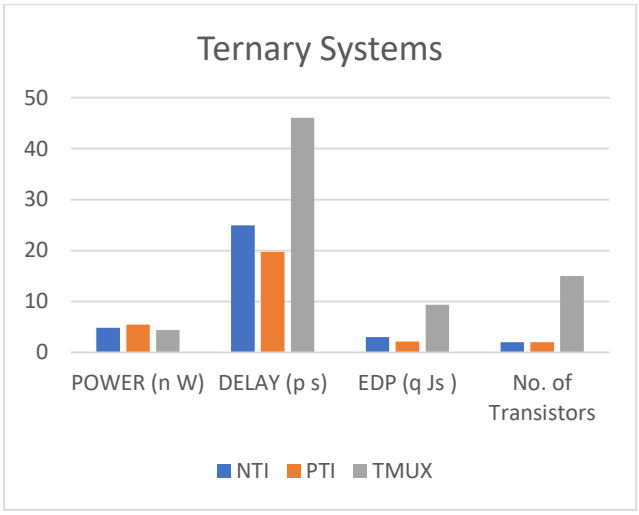


FIGURE 14. Results for Ternary Systems

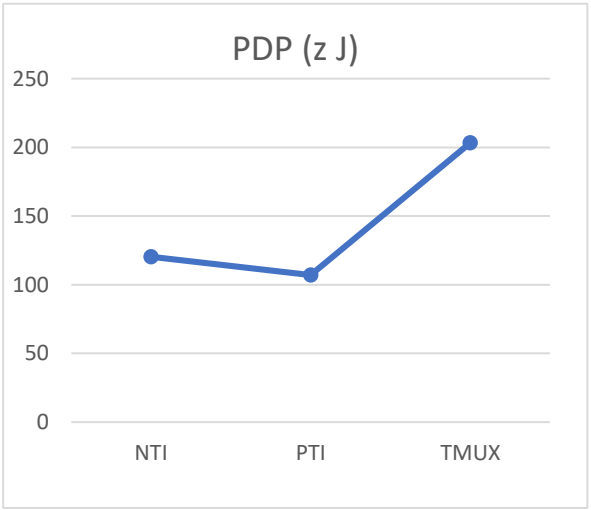


FIGURE 15. PDP for Ternary Systems

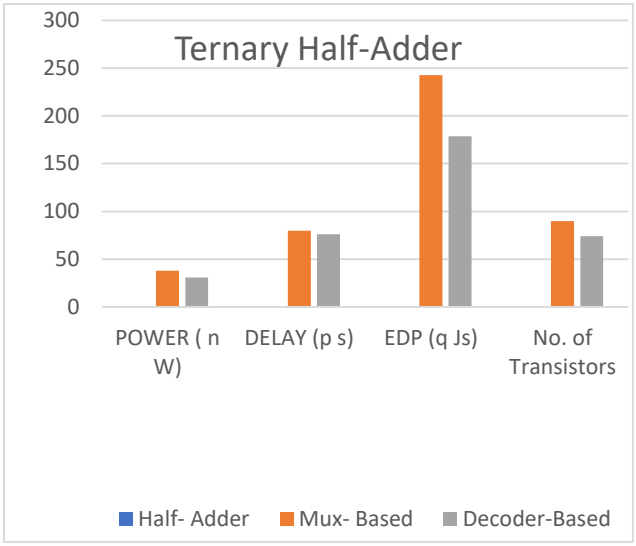


FIGURE 16. Results for Ternary Half-Adder

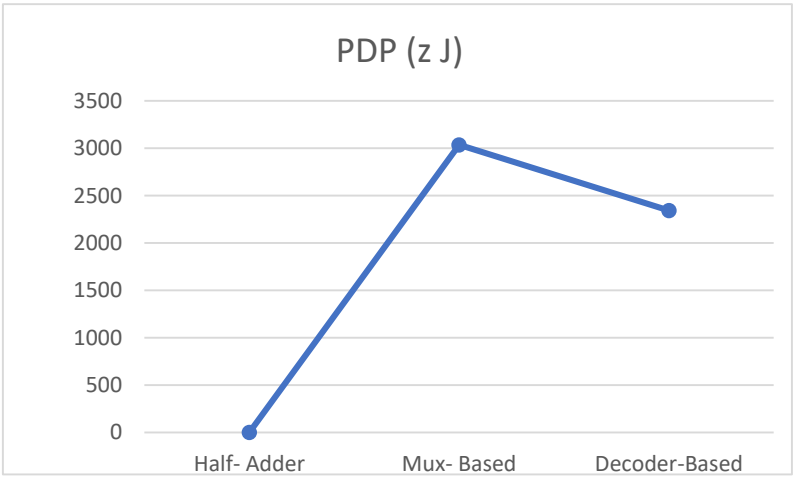


FIGURE 17. PDP for Ternary Half-Adder

The comparative analysis of ternary systems and half-adders reveals clear performance distinctions between different designs. For ternary systems, NTI and PTI demonstrate lower power consumption (4.8313 nW and 5.4381 nW, respectively) and delay compared to TMUX (4.4162 nW, 46.062 ps), but TMUX requires significantly more transistors (15 vs. 2). In ternary half-adders, the decoder-based design outperforms the mux-based approach, consuming less power (30.728 nW vs. 37.952 nW), exhibiting lower delay (76.248 ps vs. 79.957 ps), and achieving superior energy efficiency with a 22.8% reduction in Power-Delay Product (PDP) (2342.9 zJ vs. 3034.5 zJ). Additionally, the decoder-based design uses fewer transistors (74 vs. 90), making it more compact and efficient. These results highlight the decoder-based THA as the preferred choice for low-power, high-speed ternary arithmetic applications.

5. CONCLUSION

This study demonstrates that the decoder-based ternary half adder (THA) outperforms the multiplexer-based design in terms of power efficiency (30.728 nW vs. 37.952 nW), speed (76.248 ps vs. 79.957 ps), and transistor count (74 vs. 90), making it a superior choice for CNTFET-based ternary logic circuits. The decoder-based approach achieves a 22.8% improvement in power-delay product (PDP), highlighting its suitability for low-power, high-performance applications. These findings validate the potential of *CNTFET technology* in advancing multi-valued logic systems, offering a promising solution to the limitations of traditional binary designs in nanoscale computing. Future work could explore optimized ternary full adders and further scalability of CNTFET-based circuits for next-generation electronics.

REFERENCES

[1]. E. Abbasian, S. sofimowloodi, A. Sachdeva, Highly-efficient CNTFET-based unbalanced ternary logic gates, ECS J. Solid State Sci. Technol. 12 (2023) 031007.

[2]. Esmaeili, B. Bakhshi, A new BGP-based load distribution approach in geographically distributed data centers, Nashriyyah-i Muhandisi-i Barq va Muhandisi-i Kampyutar-i Iran 62 (2018) 71.

[3]. J. Zandi, A.N. Afooshteh, M. Ghassemian, Implementation and analysis of a novel low power and portable energy measurement tool for wireless sensor nodes, in: Proceedings of the Electrical Engineering (ICEE), Iranian Conference, 2018, pp. 1517–1522, on.

[4]. E. Nikbakht, D. Dideban, N. Moezi, A half adder design based on ternary multiplexers in carbon nano- tube field effect transistor (CNFET) technology, ECS J. Solid State Sci. Technol. 9 (2020) 081001.

[5]. E. Abbasian, N. Mahdiye, A high-speed low-energy one-trit ternary multiplier circuit design in CNTFET technology, ECS J. Solid State Sci. Technol. 12 (2023) 021004.

[6]. M.H. Moaiyeri, M. Nasiri, N. Khastoo, An efficient ternary serial adder based on carbon nanotube

[7]. FETs, Eng. Sci. Technol. Int. J. 19 (2016) 271–278.

[8]. E. Mani, E. Abbasian, M. Gunasegeran, S. Sofimowloodi, Design of high stability, low power and high speed 12 T SRAM cell in 32-nm CNTFET technology, AEU Int.J. Electron. Commun. 154 (2022) 154308.

[9]. Sachdeva, D. Kumar, E. Abbasian, A carbon nano-tube field effect transistor based stable, low- power 8T static random access memory cell with improved write access time, AEU Int. J. Electron. Commun. (2023) 154565.

[10]. B.D. Madhuri, S. Sunithamani, Design of ternary logic gates and circuits using GNRFETs, IET Circuits Devices Syst. 14 (2020) 972–979.

[11]. R.A. Jaber, A.M. El-Hajj, A. Kassem, L.A. Nimri, A.M. Haidar, CNFET-based designs of ternary half- adder using a novel "decoder-less" ternary multiplexer based on unary operators, Microelectron. J. 96 (2020) 104698.

[12]. T. Sharma, L. Kumre, CNTFET-based design of ternary arithmetic modules, Circuits Systems Signal Process. 38 (2019) 4640–4666.

[13]. T. Sharma, L. Kumre, CNFET based design of unbalanced ternary circuits using efficient shifting literals, Microelectron. J. 104 (2020) 104869.

[14]. F.M. Sardroudi, M. Habibi, M.H. Moaiyeri, A low-power dynamic ternary full adder using carbon nanotube field-effect transistors, AEU Int. J. Electron. Commun. 131 (2021) 153600.

[15]. J. Zandi, A. Naderi-Afooshteh, LRBAC: flexible function-level hierarchical role based access control for Linux, in: Proceedings of the 2015 12th International Iranian Society of Cryptology Conference on Information Security and Cryptology (ISCISC), 2015, pp. 29–35.

[16]. R.A. Jaber, A. Kassem, A.M. El-Hajj, L.A. El-Nimri, A.M. Haidar, High-performance and energy-efficient CNFET-based designs for ternary logic circuits, IEEE Access 7 (2019) 93871–93886.

[17]. F. Hajizadeh, M.B. Marvasti, S.A. Asghari, M.A. Mollaei, A.M. Rahmani, Configurable DSI partitioned approximate multiplier, Future Gener. Comput. Syst. 115 (2021) 100–114.

[18]. S. Tabrizchi, A. Panahi, F. Sharifi, H. Mahmoodi, A.H.A. Badawy, Energy-efficient ternary multipliers using CNT transistors, Electronics 9 (2020) 643.

[19]. K. Rajkumar, G.U. Reddy, Performance analysis of Cu-MWCNT bundled HCTSVs using ternary logic, e Prime Adv. Electr. Eng. Electron. Energy 5 (2023) 100247.

[20]. S. RatanKumar, L.K. Rao, M.K. Kumar, Design of ternary logic circuits using pseudo N-type CNTFETs, ECS J. Solid State Sci. Technol. 11 (2022) 111003.

[21]. R.A. Jaber, A.M. Haidar, A. Kassem, CNTFET-based design of ternary multiplier using only multiplexers, in: Proceedings of the 2020 32nd International Conference on Microelectronics (ICM), 2020, pp. 1–4

[22]. S. Tabrizchi, F. Sharifi, P. Dehghani, Energy-efficient and PVT-tolerant CNFET- based ternary full

[23]. adder cell, Circuits Systems Signal Process. 40 (2021) 3523–3535.

[24]. M. Rahbar, B. Li, N. Hunter, I. Al Keyyam, T. Wang, E. Shi, Observing grain boundary-induced phonons mean free path in highly aligned SWCNT bundles by low-momentum phonon scattering, Cell Rep. Phys. Sci. 4 (2023) 101688.

[25]. T. Khurshid, V. Singh, Energy efficient design of unbalanced ternary logic gates and arithmetic circuits using CNTFET, AEU Int. J. Electron. Commun. (2023) 154601.

[26]. J. Deng, H.S.P. Wong, A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part II: full device model and circuit performance benchmarking, IEEE Trans. Electron. Devices 54 (2007) 3195–3205.

[27]. J. Deng, H.-S.P. Wong, A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: model of the intrinsic channel region, IEEE Trans. Electron. Devices 54 (2007) 3186–3194.

[28]. M.H. Moaiyeri, A. Doostaregan, K. Navi, Design of energy-efficient and robust ternary circuits for nanotechnology, IET Circuits Devices Syst. 5 (2011) 285–296.

[29]. M. Glusker, D.M. Hogan, P. Vass, The ternary calculating machine of Thomas Fowler, IEEE Ann. Hist. Comput. 27 (2005) 4–22.

[30]. E. Abbasian, S. Sofimowloodi, A high-performance and energy-efficient ternary multiplier using CNTFETs, Arab. J. Sci. Eng. (2023) 1–15.

[31]. F. Zahoor, T.Z.A. Zulkifli, F.A. Khanday, S.A.Z. Murad, Carbon nanotube and resistive random access memory based unbalanced ternary logic gates and basic arithmetic circuits, IEEE Access 8 (2020)

[32]. 104701–104717.

[33]. S. Kim, S.Y. Lee, S. Park, K.R. Kim, S. Kang, A logic synthesis methodology for low- power ternary logic circuits, IEEE Trans. Circuits Syst. Regul. Pap. 67 (2020) 3138–3151.
[34]. S. Tabrizchi, N. Azimi, K. Navi, A novel ternary half adder and multiplier based on carbon nanotube field effect transistors, Front. Inf. Technol. Electron. Eng. 18 (2017) 423–433.
[35]. A.D. Zarandi, M.R. Reshadinezhad, A. Rubio, A systematic method to design efficient ternary high performance CNTFET-based logic cells, IEEE Access 8 (2020) 58585–58593.
[36]. S. Tabrizchi, M. Taheri, K. Navi, N. Bagherzadeh, Novel CNFET ternary circuit techniques for high-performance and energy-efficient design, IET Circuits Devices Syst. 13 (2019) 193–202.
[37]. J.M. Aljaam, R.A. Jaber, S.A. Al-Maadeed, Novel ternary adder and multiplier designs without using decoders or encoders, IEEE Access 9 (2021) 56726–56735.
[38]. R.A. Jaber, J.M. Aljaam, B.N. Owaydat, S.A. Al-Maadeed, A. Kassem, A.M. Haidar, Ultra-low energy CNFET-based ternary combinational circuits designs, IEEE Access 9 (2021) 115951–115961.
[39]. S. Lin, Y.-B. Kim, F. Lombardi, CNTFET-based design of ternary logic gates and arithmetic circuits, IEEE Trans. Nanotechnol. 10 (2009) 217–225.
[40]. Stanford University CNFET Model Website, Stanford University, CA, 2008 [Online] Available in, http://nano.stanford.edu/model.php?Id 23.
[41]. Y. Shrivastava, T.K. Gupta, Design of low-power high-speed CNFET 1-trit unbalanced ternary multiplier, Int. J. Numer. Model. Electron. Netw. Devices Fields 33 (2020) e2685.
[42]. H. Samadi, A. Shahhoseini, F. Aghaei-liavali, A new method on designing and simulating CNTFET_based ternary gates and arithmetic circuits, Microelectron. J. 63 (2017) 41–48.
[43]. Doostaregan, A. Abrishamifar, Evaluating a methodology for designing CNFET- based ternary circuits, Circuits Syst. Signal Process. 39 (2020) 5039–5058.
[44]. S. Musala, R.M. Gajula, S.R.S. Reddy, P.P. Reddy, High-speed low power energy efficient 1-trit multiplier with less number of CNTFETs. Multimed. Tools Appl., 2023, pp. 1–13, https://doi.org/10.1007/s11042-023-16403-9.
[45]. M. H. Moaiyeri, R. F. Mirzaee, K. Navi, and O.Hashemipour,"Efficient CNTFET- basedternary full adder cells for nanoelectronics," Nano-MicroLett., 3(1) 4350, (2011).
[46]. C. Venkataiah, Y. Mallikarjuna Rao, Manjula Jayamma, Rambabu, MK Linga Murthy, H. Laith, Alzubaidi, Sanjay Mishra, "4-Bit Ternary Adder and Multiplier using CNTFET for High Speed arithmetic circuits", E3S Web of Conferences 391, 01221(2023).
[47]. J. Srinivas Rao, Suresh Kumar Tummala, Narasimha Raju Kuthuri, Comparative investigation of 15 Level and 17 level cascaded h-bridge MLI with cross h-bridge MLI fed permanent magnet synchronous motor, Indonesian Journal of Electrical Engineering and Computer Science, 21(2), pp: 723-734, (2020)
[48]. B. Srinivasu, K. Sridharan,"A Synthesis Methodology for Ternary Logic Circuits in Emerging Device Technologies" IEEE TCAS-1, 99 ,1-14, (2017).
[49]. Tummala, S.K., Kosaraju, S. & Bobba, P.B. Optimized power generation in solar using carbon substrate for reduced greenhouse gas effect. Appl Nanosci 12, 1537– 1543 (2022).[47] M. Moaiyeri, R. Mirzaee, K. Navi, and O. Hashemipour, "Efficient CNTFETbased ternary full adder cells for nanoelectronics," Nano-Micro Lett., 3, 1, 43–50, (2011).
[50]. S. Kim, T. Lim, and S. Kang, "An optimal gate design for the synthesis of ternary logic circuits," in Proc. 23rd Asia South Pacific Design Automat. Conf. (ASPDAC), 476–481, Jan. (2018).
[51]. Suresh Kumar Tummala, Phaneendra Babu Bobba & Kosaraju Satyanarayana (2022) SEM & EDAX analysis of super capacitor, Advances in Materials and Processing Technologies, 8:sup4, 2398-2409
[52]. P. Keshavarzian and R. Sarikhani, "A novel CNTFET-based ternary full adder," Circuits, Syst. Signal Process., 33, 665–679, (2014).
[53]. C. Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "Insertion of optimal number of repeaters in pipelined nano interconnects for transient delay minimization", Cir sys and sig proc, February, (2019).
[54]. C. Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "FDTD algorithm to achieve absolute stability in performance analysis of SWCNT interconnects", Jour of comp elect, June, (2018).
[55]. Davu, S.R., Tejavathu, R. & Tummala, S.K. EDAX analysis of poly crystalline solar cell with silicon nitride coating. Int J Interact Des Manuf (2022).
[56]. S. Lin, Y. Kim and F. Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits," IEEE Trans. Nanotech, 10,217-225, March (2011).
[57]. Raychowdhury and K. Roy, "Carbon-nanotube-based voltage-mode multiplevalued logic design," IEEE Trans. Nanotech, 4,168-179, March (2005).
[58]. Tummala, S.K., Indira Priyadarshini, T., Morphological Operations and Histogram Analysis of SEM Images using Python, Indian Journal of Engineering and Materials Sciences, 2022, 29(6), pp. 794–798.
[59]. M. K. Q. Jooq, M. H. Moaiyeri and K. Tamersit, "Ultra-compact ternary logic gates based on negative capacitance carbon nanotube FETs," IEEE Trans. Circuits Syst. II, Exp. Briefs, 68,2162-2166, June (2021).
[60]. M. H. Moaiyeri, A. Doostaregan, K. Navi, "Design of energy-efficient and robust ternary circuits for nanotechnology," IET Circuits, Devices & Syst., 5, 285-296, July (2011).
[61]. C. Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "Signal integrity analysis for coupled SWCNT interconnects using stable recursive algorithm", Microelect Jour,74,13-23, April, (2018).
[62]. [60] C. Venkataiah, V.N.V. Satya Prakash, K. Mallikarjuna and T. Jayachandra Prasad, "Investigating the effect of chirality, oxide thickness, temperature and channel length variation on a threshold voltage of MOSFET, GNRFET, and CNTFET", Jour of mech of cont and math sci, 232-244, September, (2019).

[63]. Vijay Rao Kumbhare, Punya Prasanna Paltani, C. Venkataiah, and Manoj Kumar Majumder "Analytical Study of Bundled MWCNT and Edged-MLGNR Interconnects: Impact on Propagation Delay and Area", IEEE Trans on Nanotech, 18, 606-610, June, (2019).

[64]. Karthik Rao, R., Bobba, P.B., Suresh Kumar, T., Kosaraju, S., Feasibility analysis of different conducting and insulation materials used in laminated busbars, Materials Today: Proceedings, 2019, 26, pp. 3085–3089

[65]. B. Srinivasu and K. Sridharan, "A synthesis methodology for ternary logic circuits in emerging device technologies," IEEE Trans. Circuits Syst. I, Reg. Papers,64, 2146-2159, Aug. (2017).

[66]. S. Tabrizchi, A. Panahi, F. Sharifi, H. Mahmoodi, and A.-H. A. Badawy, "Energyefficient ternary multipliers using CNT transistors," Electronics, 9, 643, (2020). 17 E3S Web of Conferences 391, 01221 (2023) https://doi.org/10.1051/e3sconf/202339101221 ICMED-ICMPC 2023

[67]. K. Kim et al., "Extreme low power technology using ternary arithmetic logic circuits via drastic interconnect length reduction," Proc. IEEE 50th Int. Symp. Multiple-Valued Log. (ISMVL), 155-158, (2020).

[68]. Y. Kang et al., "A novel ternary multiplier based on ternary CMOS compact model," Proc. IEEE 47th Int. Symp. Multiple-Valued Log. (ISMVL), 25-30, (2017).

[69]. H. Sirugudi, S. Gadgil and C. Vudadha, "A novel low power ternary multiplier design using CNFETs," Proc. 33rd Int. Conf. VLSI Des. 19thInt. Conf. Embedded Syst. (VLSID), 25-30, (2020). 27. O. J. Bedrij, "Carry-Select Adder," IRE Trans. Electronic Computers,11,340-346, June (1962).

[70]. P. Keshavarzian and R. Sarikhani, "A novel CNTFET-based ternary fulladder," Circuits Syst. Signal Process. 33,665679, (2014).