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Single Stage On Board Electric Vehicle Charger with Soft Switching and High Efficiency

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Abstract: *This paper presents an innovative isolated single- stage on-board electric vehicle (EV) charger utilizing a current-source topology, eliminating the need for an intermediate DC-link. The proposed design achieves soft- switching in semiconductors across all AC line voltages and varying load conditions, optimizing efficiency and reducing switching losses. Notably, it operates without external snubber or clamp circuits, simplifying the design and improving system reliability. The charger employs phase- shift modulation for power factor correction (PFC) and voltage regulation, ensuring minimal circulatingenergy.A3 kW prototype with silicon carbide (SiC) semiconductors demonstrates peak efficiency of 96.4%, with efficiencies above 95% at maximum power and a total harmonic distortion (THD) of 4.1%.The paper includes an analysis of control strategies, component stresses, and design constraints. Experimental results validate the topology's effectiveness for real-world EV applications. Additionally, an Adaptive Neuron- Fuzzy Inference System (ANFIS) controller is proposed to further optimize performance under variable load and input conditions, enhancing power factor correction and overall efficiency for future smart EV charging solutions.*

1. INTRODUCTION

The transition to electric vehicles (EVs) is central to achieving sustainable transportation systems, reducing greenhouse gas emissions, and enhancing energy efficiency worldwide.Astheglobal market for EVscontinuesto grow, the development of efficient, reliable, and fast charging solutions become increasingly important. Efficient on-board chargers (OBCs) play a pivotal role in the successful adoption of EVs by enabling drivers to charge their vehicles quickly, safely, and without excessive energy waste. However, current charging systems face numerous challenges, particularly in terms of complexity, power losses, component stress, and system reliability. This paper introduce seen in no vativeisolated single-stage on- board charger that uses a current-source topology, designed to overcome these challenges and optimize the overall performance of electric vehicle charging systems. Unlike traditional multi-stage designs, which often involve an intermediate DC-link and additional snubbed or clamp circuits, the proposed charger offers as amplified solution with enhance deficiency and reduced component stress. By using a current-source converter, the system achieves soft- switching Capabilities across a wide range of AC line voltages and varying load conditions, which significantly reduces switching losses and enhances overall system efficiency. The increasing demand for high-performance EV chargers necessitates continuous innovations in power electronics, especially in terms of maximizing energy efficiency while minimizing the physical footprint and cost of components. One of the most important in modern charging systems is to minimize power losses, particularly in the form of switching losses in semiconductors. Switching losses can become significant, especially at higher power levels and under varying operational conditions, such as the audience's input voltage is raised. The provost is charged Addresses this by employing a current-source topology that enables soft-switching across the entire AC line voltage range, ensuring that energy is delivered efficiently while minimizing losses. A key challenge in designing EV chargers is maintaining high efficiency while also managing power factor correction (PFC) and voltage regulation. Conventional designs often rely On complex modulations chimes and auxiliary circuits to ensure that the system operates efficiently under different loads. However, these techniques can introduce additional complexity, reduce system reliability, and increase the

overall cost of the system. The proposed charger uses a straight forward phase-shift modulation technique to accomplish both PFC and voltage regulation, minimizing circulating energy within the system. This approach ensures optimal operation under aide range of conditions, providing excellent performance in terms of both charging speed and energy efficiency. One of the defining features of the proposed system is its exceptional efficiency, especially in constant power charging mode. Experimental results from a 3 kW prototype using advanced silicon carbide (SiC) semiconductor devices demonstrate a peak efficiency of 96.4%. This level of efficiency is highly significant for the EV market, where even small improvements in charger performance can have a substantial impact on overall energy savings and environmental sustainability. Moreover, the charger maintains efficiencies above 95% even during operation at maximum power, with total harmonic distortion (THD) of 4.1%, which is well within acceptable limits for most grid- connected systems. A major advantage of the proposed design is the elimination of external snubbed or clamp circuits, which are commonly used In Traditional EV charger Store duce switching spikes and manage voltage transients. By eliminating the subcomponents, the system not only simplifies the overall design but also reduces the stress on key components such as the semi the conductive switches contribute to higher reliability and longer system lifetime. This simplified approach also leads to reduced manufacturing costs and reduced maintenance costs over the operational life of the system. The proposed charger design also focuses on the control system, which plays a key role in ensuring that the system operates at peak performance and reliability. This paper presents a detailed analysis of the control strategies used in the charger, including the handling of component stresses and design constraints considered during development. These strategies aim to strike a balance between performance and reliability, ensuring that the charger operates efficiently under real-world conditions. Beyond the basic design improvements, this paper also explores the integration of an adaptive neural-fuzzy inference system (ANFIS) controller to further improve the charger's performance under varying operating conditions. ANFIS, which combines the key advantages of neural networks and fuzzy logic, is a promising approach for managing complex, nonlinear systems ANFIS controller can adapt to the charger load demand and fluctuations in input voltage, providing improved power factor correction, reducing circulating energy, and further improving the overall system efficiency. The potential for adaptive control techniques such as ANFIS in EV charging systems represents an exciting area for future research and development. By introducing smart and adaptive control mechanisms, the charger can dynamically adjust to changing conditions, providing improved energy savings, lower costs, and improved reliability. These findings could significantly contribute to the continued development of smart charging solutions, which are expected to become increasingly important as the number of electric vehicles on the road continues to grow. In summary, this paper presents an innovative isolated single-stage on-board charger with a current-source topology that achieves significant improvements in efficiency, simplicity, and reliability. By using soft-switching techniques, eliminating the need for external snubbed circuits, and using a direct modulation scheme for power factor correction and voltage regulation, the proposed charger takes a step forward in the design of next-generation EV charging systems. Experimental results show that this system achieves 96.4% speech efficiency, High performance under various load conditions. The integration of the ANFIS controller provides the ability to adapt the system to dynamic charging environments and further optimize it. The work presented here lays the foundation for developing intelligent, efficient and cost-effective charging solutions that will play a key role in the widespread adoption of electric vehicles.

2. PROPOSEDOBCTOPOLOGY

This section describes the proposed current source topology for EVOBC. It does not require external clamp circuits, and only two inverter transistors need to have reverse voltage blocking capability. OBC topologies are shown in Figure.2 uses two magnetic elements, providing smooth-switching for the transistors over the entire input voltage range and a constant switching frequency regardless of the converter gain requirements. The switching power required for smooth-switching is controlled based on the instantaneous value of the input current. This feature also reduces conduction losses in the converter due to reduced cycling energy resulting from input voltage variation or light load operating conditions. Lossless snubbed capacitors are used in the secondary devices to reduce dv/dt switching and turn-off losses [29], [30].

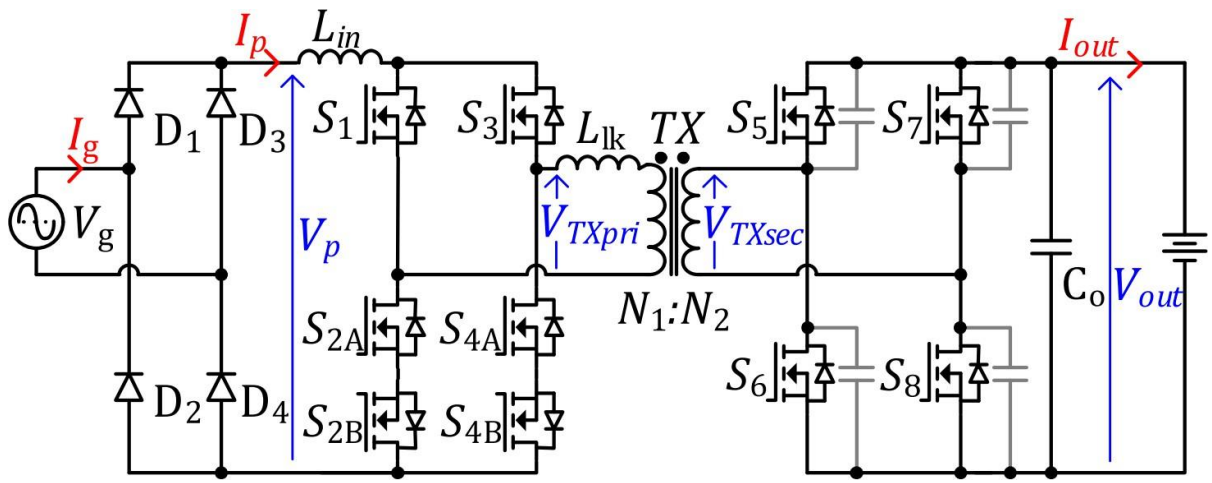

FIGURE 1. Proposed AC-DC current source on board charger.

A. Operation Principle

The grid voltage V GIs rectified to unipolar pulsating voltage Vp utilizing the diode bridge D1-D4.The input rectifier could consist of passive diodes for unidirectional charging applications or active switches for bidirectional energy flow. The following analysis assumes that the components are ideal and lossless. The effect of magnetizing inductance of the transformer TX is not taken into account, as it is not utilized in the proposed modulation method. The unipolar pulsating voltage VP applied to the A-SMC converter is assumed to be constant for the switching period Tsw. The input unipolar pulsating current Ip flows through the inductor Lin that provides energy storage for boost operation and acts as the input filter of the converter .Further ,the energy is transferred to the load, utilizing a full-bridge inverter, a high frequency transformer, and a rectifier. The generalized switching waveforms of the converter are presented in Fig. 3. Interval 1 [t0 — t1]: The equivalent circuit of this interval is shown in Fig. 4(a). At the instant t0, the inductance Lin is energized. The sum of the input voltage and the voltage of the inductor Lin is applied to the primary winding of the transformer. The converter is operating in the active state, and the energy is transferred to the load. Interval 2 [t1 — t2]: It begins with the turn-off of the switch S4Bandturn-onofS2A, asshowninFig.4 (b). The current Flows through the bridge leg S1, S2A, and S2B, energizing the input inductor. Body diode of the transistor S4Bprevents short-circuit of the transformer primary winding and blocks the prohibited current path. The energy flow through the switchS4Adecaysnaturally, which allows for the turn-off of the transistor with zero current switching (ZCS). Interval 3 [t2 — t3]: The current continues flowing through the bridge leg, energizing the inductor (Fig. 4(c)). The duration of this interval is a control variable that determines the amount of energy to be stored in the inductor. Interval 4 [t3 — t4]: At the instant t3, transistor S3 is turned on (Fig. 4(d)). The primary winding of the transformer is shortcircuitedthroughS1andS3.SwitchesS5andS8arealso turned on. Hence, the current flows through the output switchesS5andS8, transformer TX, and switches S1andS3. The current slope di/dt is limited by the transformer leakage inductance. The peak value of the transformer current is determined byte duration of this state, which is terminated byturningoffswitchesS5andS8.Atthesametime, the input current and the transformer current are flowing in the oppositedirectionintheswitchS1.At the instant t4,the sum of the secrets equals zero ,which allows for soft turn-off of The transistor. The transformer current should reach a slightly higher value than the instantaneous value of the grid current to ensure ZCS. Interval 5 [t4 — t5]: The snubbed capacitances of the secondary side transistors and leakage inductance create a small resonant tank. Thus, after turning off switches S5 and S8, The resonant current is still flowing through the same path, as shown in Fig. 4(e).At the instant t5, the switch S1should be turned off. Practically, S1 is turned off earlier to ensure safe operation and part of the resonant tank energy is transferredthroughthebodydiodeofS1.Aftertheinstantt5, the transient process ends, the current through the switch S1 reduces to zero, and the parasitic capacitances on the secondary side are recharged. The converter begins delivering energy from the grid side to the battery in the active state using another switching diagonal, as shown in Fig. 4(f). Based on the above-mentioned switching states, the following variables are critical for further analysis: switching period of the converter Tsw; on-state duty cycle of the primary-side bridge switches DA; on-state duty cycle of the secondary-side bridge switches DT; the duty cycle of the shoot-through state D, which is determined by the phase-

shift between the switches.

B. Design Considerations

The OBC design is based on the assumption that RMS grid voltage varies in the range of Vg (RMS) = 200…253 V, and the battery voltage is in the range of V out = 330…470 V.A two- Step charging method is used. First, the battery is charged. With the constant input power (CP mode) of Pin =3kW, until the battery voltage reaches its maximum value V out (max) = 470V.In these Cond charging step, the constant voltage (CV) mode is used. The transformer turns ratio should provide Proper operation of the converter at the Vg peak value, while the output voltage V out is minimal. The minimal gain of the converter is similar to the conventional boost converter, and the transformer turns ratio n (N2/N1) can be estimated as follows:

$$n = \frac{V_{out(\min)}}{V_{g(\max)} \cdot \frac{1}{1-D_{\min}} \cdot \eta},$$

Where D min is the minimum possible duty cycle D of the converter and η is the efficiency of the converter. The minimum value of D minisde fined by the interval duration of the transistor soft commutation t12, t34, t45:

$$t_{12} \approx t_{34} = \frac{n \cdot I_p}{V_{out}} \cdot L_{lk},$$

Where Tsw is the switching period. The duration of falling and rising edges of the current pulse t12 and t34, respectively, are defined as follows:

$$D_{\min} = \frac{2 \cdot (t_{12} + t_{34} + t_{45})}{T_{sw}},$$

And the resonant interval duration 45i s:

$$t_{45} = \frac{1}{\omega_{res}} \cdot \arccos\left(\frac{(I_p \cdot \rho)^2 - V_{out}^2/n^2}{(I_p \cdot \rho)^2 + V_{out}^2/n^2}\right)$$

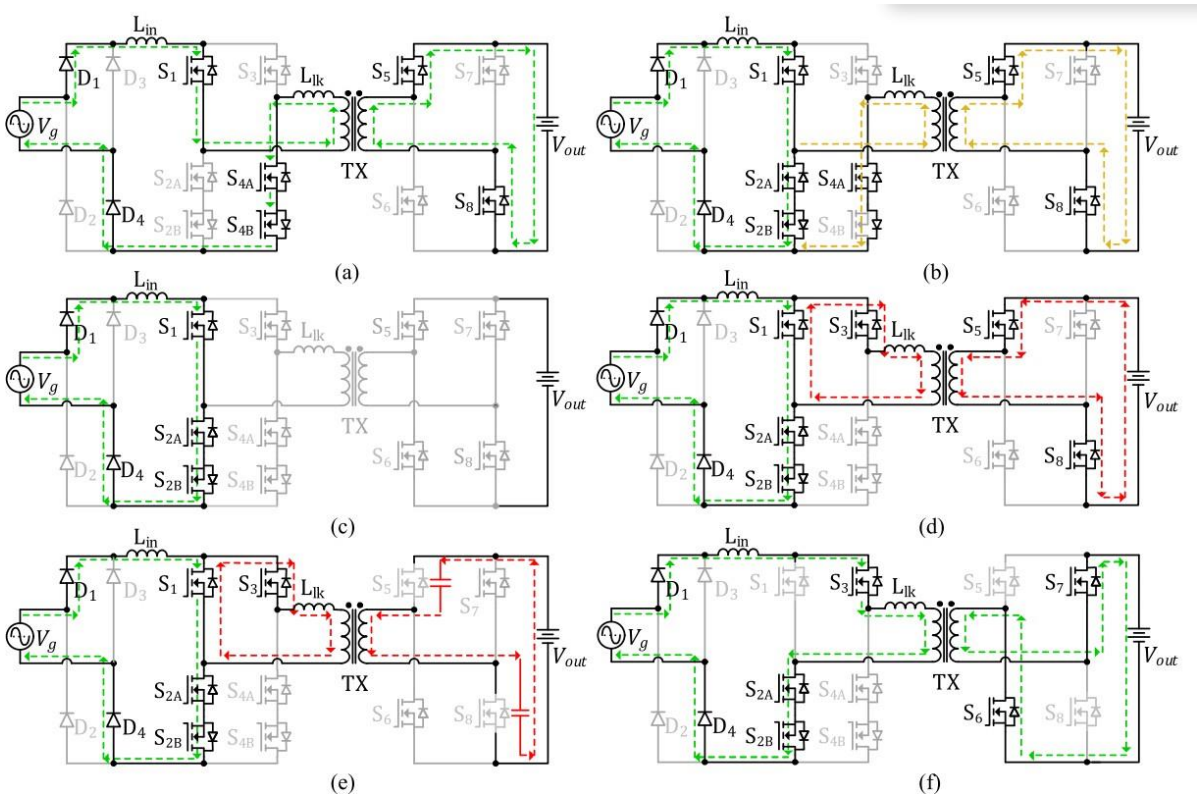

FIGURE 2.

Fig. 2. Operational states of the proposed converter :(a) Interval 1[t0—t1]; (b) Interval 2[t1—t2]; (c) Interval3 [t2 —t3]; (d) Interval 4 [t3 —t4]; (e) Interval 5 [t4 —t5]; (f) Active state, equal to Interval 1.

Where $\omega_{res} = 1/\sqrt{L_{lk} \cdot C_{spar} \cdot n^2}$ ·n² is the resonant angular frequency, $\rho = \sqrt{L_{lk}/n^2 \cdot C_{spar}}$ is the Characteristic impedance of the resonant tank, which is mostly formed by the transformer leakage inductance Llk and total equivalent circuit capacitance C_{spar} (includes parasitic capacitances of the transformer, transistors, PCB, and external snubbed capacitance).The maximum duration of t45 is achieved when the grid voltage crosses zero; in this case, (2) is simplified as:

$$D_{\min} = \frac{2 \cdot \pi}{T_{sw} \cdot \omega_{res}} = \frac{2 \cdot \pi \cdot n\sqrt{L_{lk} \cdot C_{spar}}}{T_{sw}}.$$

Based on (1) and (5), D min and n may be estimated as follows:

$$n = \frac{T_{sw} \cdot V_{out(\min)}}{V_{g(\max)} \cdot T_{sw} \cdot \eta + 2 \cdot \pi \cdot V_{out(\min)} \sqrt{L_{lk} \cdot C_{sp}}}$$

$$D_{\min} = \frac{2 \cdot \pi \cdot V_{out(\min)} \sqrt{L_{lk} \cdot C_{spar}}}{V_{g(\max)} \cdot T_{sw} \cdot \eta + 2 \cdot \pi \cdot V_{out(\min)} \sqrt{L_{lk} \cdot}}$$

As the steady-state voltage stress of the primary-side transistors equals V out /n, the turns ratio should be maximized, whereas D − minimized. Hence, the resonant frequency ωres should be maximized, or the transformer leakage inductance L_{lk} and total equivalent capacitance C_{spar} minimized. The C_{spar} and Llk boundary values for

minimizingDminareshowninFig.5.Basedontheestimated transformer leakage inductance of Llk = 5 μH and n = 0.97 determined with (6) and the case study output and input voltages, these parameters are estimated at Cspar = 1nFand D min = 0.021.

FIGURE 3.

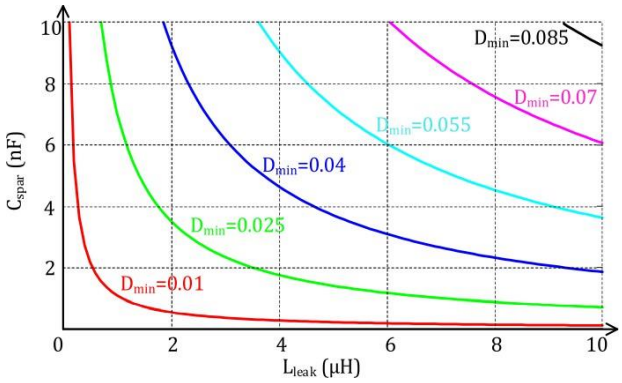

Fig. 3. The dependencies between capacitance of S5-S8 (Cspar), the transformer leakage inductance (Lleak), and the minimal duty cycle (D min). For the resonant angular frequency ω_{res} much higher than the switching ωsw, ωres >> ωsw, currents of the transistors and the transformer during the intervals t34 and t45 have minor impact on the rms current values. Therefore, they may be estimated in the same way as for conventional current -source inverters. The rms value of the transformer primary winding current ITX pri (RMS):

$$I_{TXpri(RMS)} = \frac{I_{g(\max)} \cdot V_{g(\max)} \cdot n}{V_{out}} \sqrt{\frac{1}{\pi} \cdot \int_0^{\pi} \sin(\varphi)^4 d\varphi}$$

$$= \sqrt{\frac{3}{2}} \cdot \frac{I_{in(\max)} \cdot V_{in(\max) \cdot n}}{2 \cdot V_{out}}. \qquad (8)$$

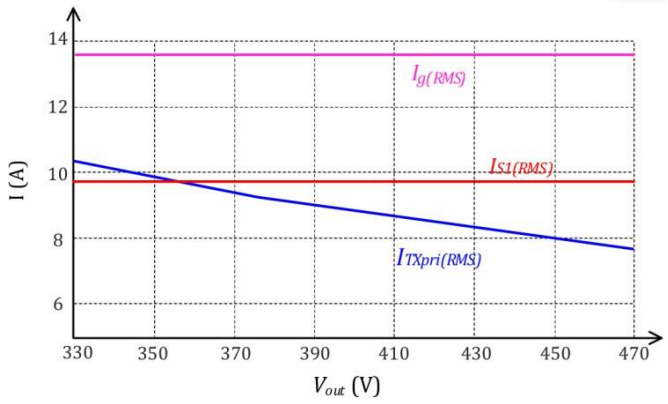

FIGURE 4.

Fig. 4. Dependence between transformer primary winding RMS current ITXpri (RMS), primary transistor S1 RMS current IS1 (RMS), and the maximum input current Ig (RMS) vs. output voltage at a constant output power. Where ϕ is the grid angle that corresponds to the fundamental angular frequency. ThermscurrentofthetransistorsS1-S4 (IS1-S4rms) is equal to:

$$I_{\mathrm{S1-S4(RMS)}}=\sqrt{\frac{1}{2\pi}\cdot\int_{0}^{\pi}\left(I_{g(\max)}\cdot\sin(\varphi)\right)^{2}d\varphi}=\frac{1}{2}\cdot I_{g(\max)}$$

The rms current of the transistors S5-S8 (IS5-S8 (RMS)) is estimated as follows:

$$I_{\mathrm{S5-S8(RMS)}}=\frac{I_{TXpri(\mathrm{RMS})}}{\sqrt{2}\cdot n}=\frac{\sqrt{3}\cdot I_{g(\max)}\cdot V_{g(\max)}}{4\cdot V_{out}}.$$

Fig. 6 shows the currents ITXpri (RMS) and ILlk (max) as functions of the output voltage. Currents in transistors S1-S8 could be derived from those values and used for the transformer design and transistor selection. The input inductor Lin should be dimensioned based on the desired THD value, which depends on the charging conditions, i.e., battery voltage and charging current. Obviously, with the state of charge rise, the current pulsations increase, which worsens the THD, particularly in the CV mode. However, for the CV mode, the power consumption is low; as a result, the impact on the grid is relatively small. Therefore, the goal is to determine the L_{in}value for sufficient THD max in the CP mode. For the THD calculation, the grid current Ig is presented as a sum of two components: fundamental sine current Iinp and ripple current component I dist:

$$I_g(\varphi)=I_{g(\max)}\cdot\sin(\varphi)+I_{dist}(\varphi).$$

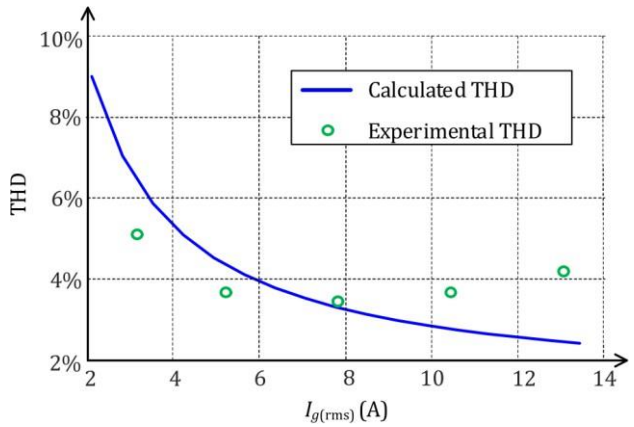

FIGURE 5.

For such model of the input current, THD is calculated as follows:

$$THD=\frac{\sqrt{2}\cdot I_{dist(\mathrm{RMS})}}{I_{in(\max)}},$$

Calculated using (13), shown at the bottom of this page. The theoretical values at V out = 400 V are presented in Fig. 7. The input inductor is calculated for the pride fined THD nom value at the end of the CP mode at the maximum voltage of the battery V out (max),where the current pulsation reaches its maximum value that could be calculated as shown in (14) at the bottom of this page. For the condition with a minimum amplitude of the grid current Iin (max)

=16.7A, Vout (max) =470V, VIN (max) = 357VandTHDnom= 3%, the inductance value equal to Lin =1.8m His obtained from (14). C. Soft-Switching Constraints For the correct operation of the converter, several criteria need to be met. As was mentioned, the ZCS is provided when the current in the primary side reaches the instantaneous input current value ip during t34. The duration of t34 can be controlled by adjusting the duty cycles of the primary transistors S1, S2

$$I_{dist(RMS)} = \sqrt{\frac{2}{\pi} \cdot \left(\int_0^{\pi/2} I_{dist}(\varphi)^2 d\varphi \right)} = \sqrt{\frac{2}{\pi} \cdot \left(\frac{1}{12} \cdot \int_0^{\pi/2} \left(\frac{V_{g(\max)} \cdot \text{si}}{L_{in}} \right.} \right.$$

$$= \frac{T_{sw} \cdot V_{g(\text{ma}}}{}$$

$$L_{in} = \frac{T_{sw} \cdot V_{g(\max)} \sqrt{9 \cdot n^2 \cdot \pi \cdot V_{g(\max)}^2 - 64 \cdot n \cdot V}}{12 \cdot \sqrt{\pi} \cdot V_{out(\max)} \cdot I_{in(\text{ma}}}$$

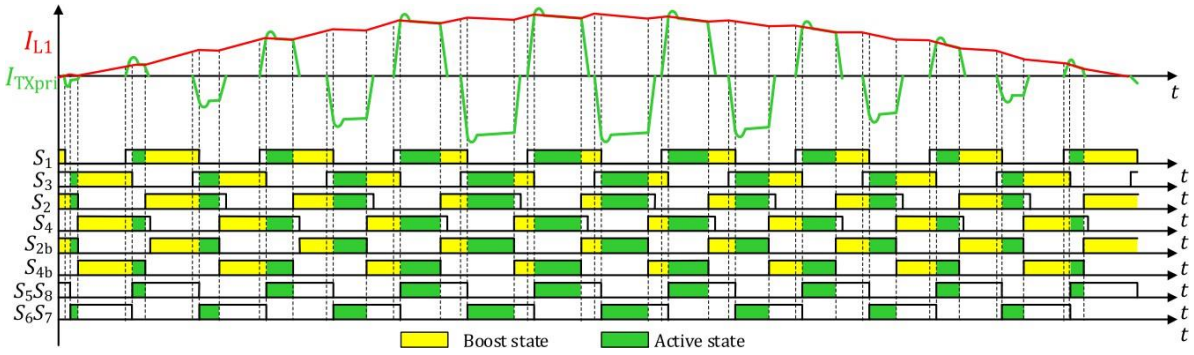

FIGURE 6 .Theoretical switching states of transistors and theoretical wave forms of the proposed converter

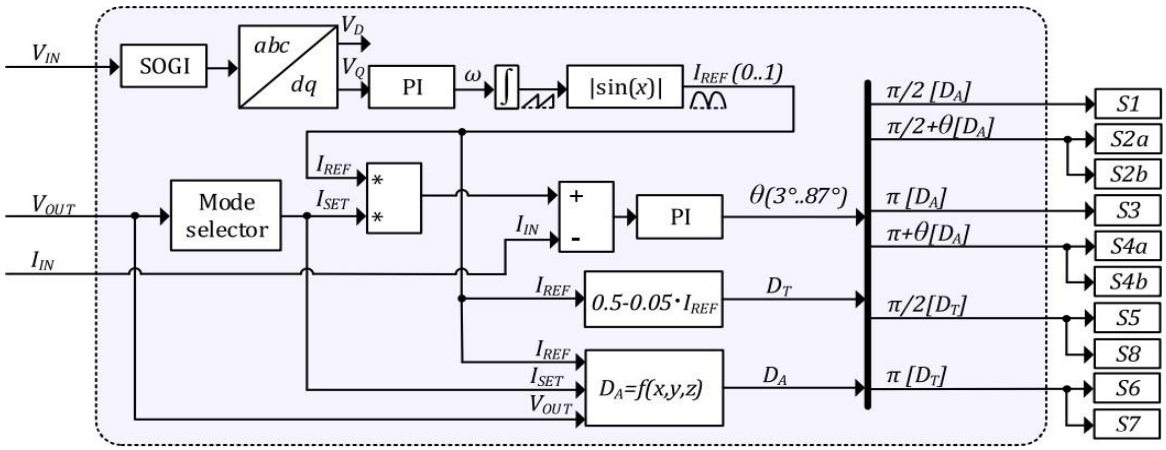

FIGURE 7. Control system of the proposed converter. S3, andS4, which can be estimated from

$$D_A \approx \frac{1}{2} + \frac{2 \cdot n \cdot i_p \cdot L_{lk}}{V_{out} \cdot T_{sw}}.$$

The duty cycles of these condary devices S5-S8 need to take into account the recharge duration of Cspar:

$$D_T < \frac{1}{2} - \frac{t_{45}}{T_{sw}}.$$

The transistors S2b and S4b operate in the synchronous rectification mode, and their duty cycle can be kept at 0.5. Moreover, the minimal phase shift angle should be set in accordance with D min using (7). As long as the conditions addressed above are satisfied, the converter will operate as intended, and the ZCS of the primary devices along with zero voltage switching (ZVS) and the soft turn-off of the secondary devices is achieved.

D. Control Strategy

The generalized switching waveforms over the grid frequency half-period are shown in Fig.6.Thesimplephase- shift modulation is used to provide sinusoidal current wave- shaping. The control system of the charger utilizes three input Signals: grid voltage, reference input current, and output voltage.ThecontrolsystemisdepictedinFig.9.Gridvoltage measurement is processed with a second-order generalized integrator phase lock loop (SOGI-PLL) to extract the fundamental frequency and the angle of the grid. Using the information acquired, normalized unipolar half-sine reference IREF is generated. Based on the battery voltage measurement, the CP or CV mode is selected, which provides the required peak current value ISET that is multiplied by the normalized reference. The resulting reference is compared with the measured current, and the obtained error signal is processed by the PI controller. The controller output is the phase-shift angle θ between current-side bridge switches, which defines the shoot-through D corresponding to the interval t1-t5. The phase-shift angle limits are applied based on (7). The resulting phase-shift angle from the controller and normalized reference information is used in the PWM generation to provide circulating energy regulation over the grid period. The phase-shift between the input bridge upper transistors and Output Bridge remains constant, while the phase-shift of the four-quadrant switches S2 and S4 is varying. The switches S2b and S4b operate in the synchronous rectification mode and could be gated complementarytoS4AandS2A, respectively. The duration of the required induced pulse for implementing the soft- switching feature depends on many factors according to (3) and (4). For the converter parameters listed in Table II and Table III, the duty cycle of the shoot-through state, hence the duty of the soft-switching pulse is simplified as:

$$D_A = \frac{2 + I_{SET}/4 + I_{REF}\left(I_{SET}/1.2 + (470 - V_{OUT})/14\right)}{3000}.$$

The denominator is equal to the carrier wave timer period counter utilized in the MCU timer peripheral. The duty cycle of primary devices is varying over the input voltage period together with phase-shift angle, which makes the soft- switching current pulse slightly higher than the steady-state transformer current. The dead-time of the secondary devices is also slightly varying depending on the instantaneous input voltage.

Adaptive Neuron-Fuzzy Inference System (ANFIS) for System Optimization

While the control strategies discussed above are essential for achieving baseline performance, further optimization can be achieved by incorporating intelligent control systems that adapt to dynamic operating conditions. This is where the Adaptive Neuron-Fuzzy Inference System (ANFIS) comes into play. ANFIS is a hybrid control technique that combines the strengths of both neural networks and fuzzy logic. Neural Networks excel at handling large amounts of data and learning from experience, while fuzzy logic is effective at making decisions in uncertain or imprecise environments. By combining these two approaches, ANFIS can model complex, nonlinear systems more accurately than traditional control techniques. In the context of the proposed EV charger, an ANFIS c varying operational conditions. EV chargers often operate in fluctuating environments, with input voltage and load demands changing over time. These variations can lead to inefficiencies if the system cannot adjust dynamically to maintain optimal performance. The integration of an ANFIS-based controller allows the charger to continuously monitor and adapt to

these fluctuations, ensuring that power factor correction, voltage regulation, and overall system efficiency are maintained at optimal levels. Specifically, the ANFIS controller can make real-time adjustments to the phase-shift modulation and other control parameters, reducing energy losses and improving efficiency during periods of high or low load. One of the primary benefits of the ANFIS controller is its ability to learn from past operating conditions and adjust its parameters accordingly. This allows the charger to operate more efficiently in varying load and input voltage conditions, which is crucial for real-world applications where these factors are not constant. By incorporating adaptive control, the charger is able to reduce circulating energy within the system and ensure that the charger operates in the most efficient mode possible, regardless of external variations. Additionally, ANFIS can improve the power factor correction (PFC) process by continuously optimizing the timing of the switching signals based on real-time data, further enhancing "The quality of the current waveform drawn from the grid optimization also helps reduce harmonic distortion, ensuring that the charger complies with grid standards and contributes to overall grid stability.

Enhanced System Efficiency and Performance

The integration of the ANFIS controller significantly enhances the overall efficiency and performance of the charger. Through continuous monitoring and real-time adjustment, the system can adapt to fluctuating load conditions, reducing power losses and improving energy utilization. This results in a more efficient charging process, reducing the overall energy consumption of the system and contributing to sustainability goals by minimizing wasted energy. The ANFIS controller's ability to optimize performance in real time also extends to improving the reliability of the system. By adapting to varying operational conditions, the controller can prevent component stress from reaching critical levels, thereby extending the life of the charger and reducing the likelihood of failures. This is particularly important in EV chargers, where continuous, reliable operation is essential for the long-term success of the technology.

Future Directions and Potential Enhancements

While the current implementation of the ANFIS controller has already shown significant improvements in the efficiency and performance of the charger, there is ample room for future improvements. As the field of machine learning and artificial intelligence advances, more sophisticated control algorithms can be developed to improve system performance. For example, the use of deep learning techniques will allow the system to predict and adjust for long-term load trends and input voltage fluctuations, resulting in more accurate control. Furthermore, the charger can communicate with the grid more effectively by integrating communication technologies such as vehicle-to-grid (V2G) or grid-to-vehicle (G2V) communication. In such a scenario, the ANFIS controller can be improved to improve the energy transfer between the vehicle and the grid, contributing to a better, more sustainable energy system.

Mathematical Analysis of the Proposed On-Board EV Charger

The mathematical analysis of the proposed on-board electric vehicle (EV) charger involves modeling the key components of the system, analyzing their operation, and deriving expressions for the performance characteristics of the system, including efficiency, power factor correction (PFC), and voltage regulation. This analysis serves as a foundation for understanding how the charger operates and optimizes the energy delivery from the AC grid to the vehicle battery.

1. Power Conversion and Current-Source Topology

The proposed charger uses a current-source topology, which means that the primary goal of the converter is to regulate the output current while maintaining minimal variations. The topology can be modeled as a power converter with an input AC source, a rectifier stage, an aDC-DC converter, and an output battery, where the converter adjusts the current according to the charging requirements of the EV's battery. The key equation governing the power conversion in a typical isolated converter is:

$$P_{in} = V_{in} I_{in} \cdot \cos(\phi)$$

Where:
• P_in is the input power (W)
• Vin is the input AC voltage (V)
• I in is the input current (A).
• ϕ is the phase angle between the input voltage and current
In a current-source topology, the current at the output is controlled, and the voltage at the output can vary depending on the load and input voltage. The system has a high power factor, meaning the current waveform should be nearly in phase with the input voltage. The power supplied to the battery:

$$P_{out} = V_{out} I_{out}$$

Where:
• Pout is the output power delivered to the battery (W).
• V out is the output voltage at the battery (V).
• I out II out is the output current (A)
For high efficiency, the power conversion process should minimize losses, which requires soft-switching operation in the semiconductor devices.

2. Soft-Switching and Switching Losses

In conventional converters, semiconductor devices experience hard-switching, where voltage and current spikes occur during switching transitions, causing losses. These losses can be reduced by using soft-switching techniques, where switching transitions occur with zero voltage or current. The mathematical analysis for soft-switching conditions can be obtained in terms of the resonant frequency and switching times of the converter.
The switching loss for a hard-switching device is usually expressed as:

$$P_{switch} = \frac{1}{2} V_{ds} I_{ds} f_{sw}$$

Where:
• Ps witch is the switching gloss (W)
• V ds is the drain-source voltage across the switch (V).
• I ds is the drain-source current through the switch (A)
• fsw is the switching frequency (Hz).
In a soft-switching converter, the switching loss is significantly reduced because the voltage or current is zero at the time of the switching event. The best soft-switching condition is achieved when the voltage across the switch is zero at the moment of the current change, which minimizes the losses.

3. Power Factor Correction (PFC)

Power factor is a measure of how efficiently the charger uses input power, and is defined as the cosine of the phase angle between the input voltage and current:

$$PFC = \cos(\phi)$$

To achieve power factor correction, the charger uses a phase-shift modulation technique. The modulation adjusts the timing of the switching signals to ensure that the current drawn from the AC grid is in phase with the AC voltage. The instantaneous power delivered to the grid can be expressed as:

$$P_{instantaneous}(t) = V_{in}(t) I_{in}(t)$$

The average input power, which corresponds to the real power, is:

$$P_{avg} = \frac{1}{T} \int_0^T P_{instantaneous}(t)dt$$

TTT duration of the input waveform. The phase-shift modulation technique adjusts the switching of the converter to align the current waveform with the voltage waveform. For optimal PFC, the average power should closely follow the input voltage waveform, and the total harmonic distortion (THD) should be minimized.

Adaptive Neuron-Fuzzy Inference System (ANFIS) Control

The application of ANFIS in the charger enables adaptive optimization of control parameters to achieve optimal performance under varying load and input conditions. ANFIS can be used to fine-tune the phase-shift modulation and power factor correction to reduce energy losses and improve the adaptive capacity of the system. The ANFIS controller adjusts the parameters based on real-time input conditions, and the learning process can be represented as:

$$f_{\text{ANFIS}} = f(\mathbf{X}, \theta)$$

Where:
• finish_ {\text{ANFIS}}fancies is the output of the ANFIS controller (adjusted modulation parameters)
• X\math{X} X is the input vector containing the system states (e.g., load, voltage)
• θ\theta are the parameters learned by the ANFIS during the training process
The ANFIS controller continuously adapts to changing load and input voltage, optimizing the switching parameters to minimize losses and maintain optimal efficiency. This adaptive nature is key to improving the overall efficiency and reliability of the charger. The proposed EV charger with current-source topology represents a significant advance in the design of efficient, reliable, and adaptive charging systems. The mathematical analysis of the charger includes key aspects of power conversion, soft-switching operation, power factor correction, efficiency calculation, and total harmonic distortion. The introduction of the ANFIS controller further improves the performance of the system by dynamically adjusting the control parameters to improve efficiency and reliability under varying operating conditions. Through these mathematical models and optimization techniques, the proposed charger achieves peak efficiency and demonstrates a robust solution for the next generation of EV charging systems.

3. RESULTS

A 3-kW OBC prototype (Figure 10) was developed to verify the topology operation and theoretical analysis presented above. The main converter components and converter parameters are listed in Table II and Table III. The transformer turns ratio is chosen to allow OBC operation at a minimum output voltage of 330VDC when a maximum grid voltage of 253 VAC is applied to the converter input. The input capacitor was designed using two T300-52Dtoroid powder cores from Micro metals. The winding consists of two parallel layers of solid copper wire, with inner and outer diameters of 1.5 and 1.25 mm, respectively.

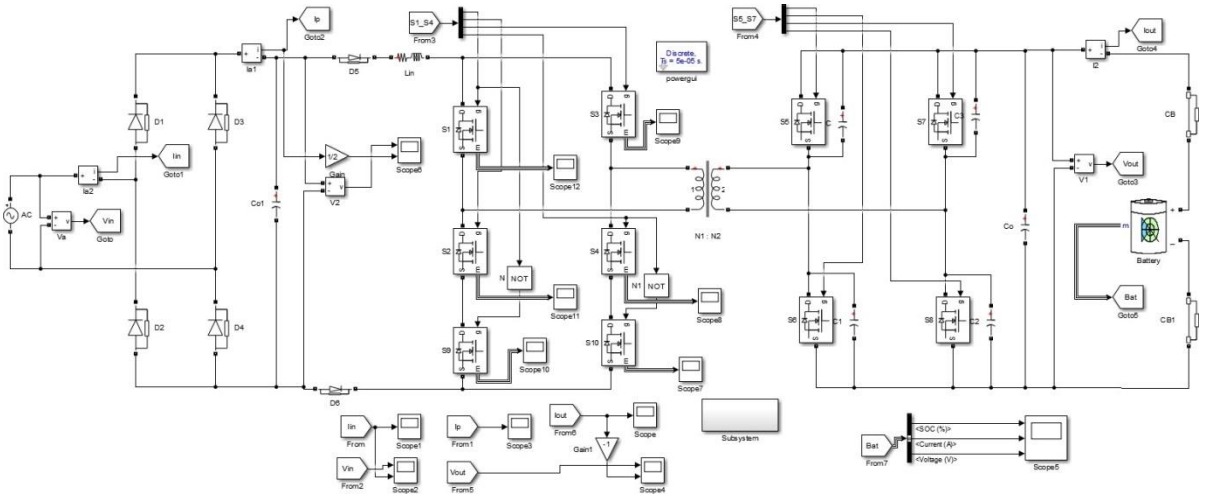

FIGURE 8. Simulation Diagram of the proposed converter.

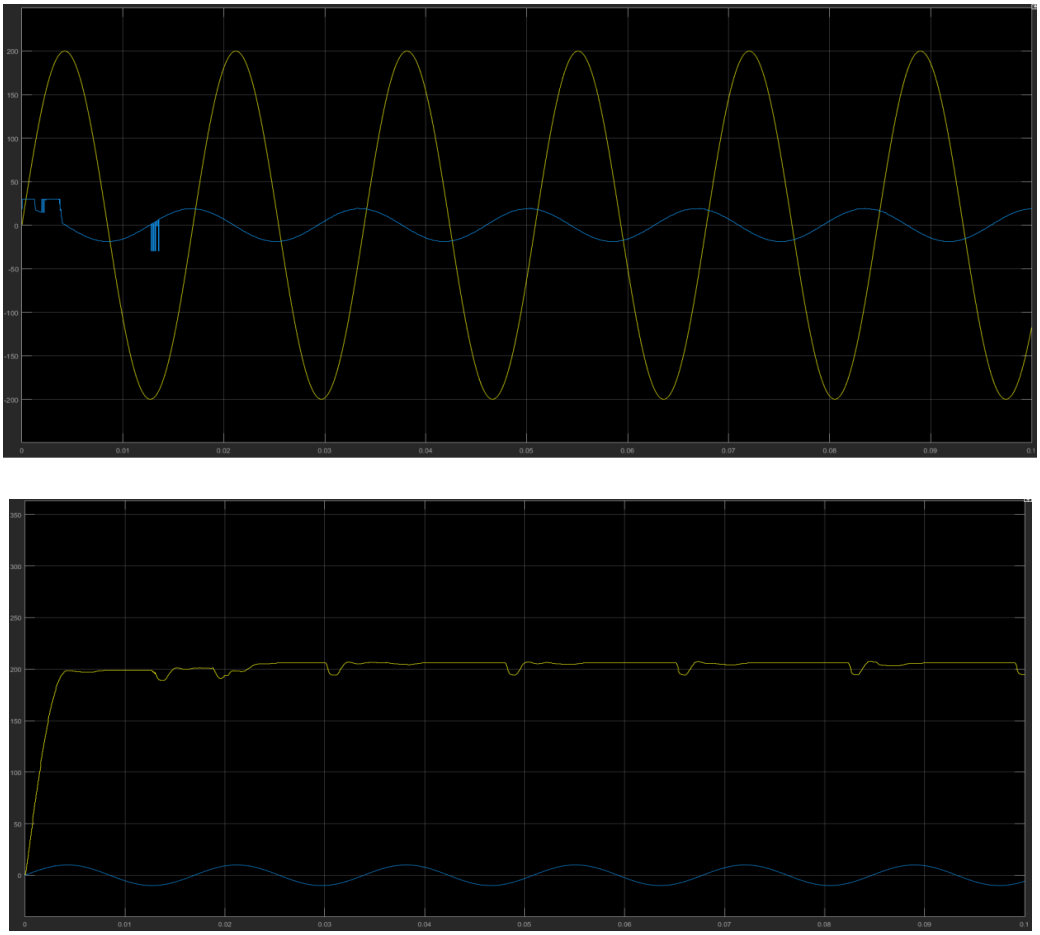

FIGURE 9.

(a) Input and output converter voltage and current in light-load operation Pin=0.8 kW, voltage=400 V; (b) Input and output converter voltage and current in full-load operation Pin=3 kW, voltage=400 V; (c) Converter reference step-mem dynamic response Vout=400 V

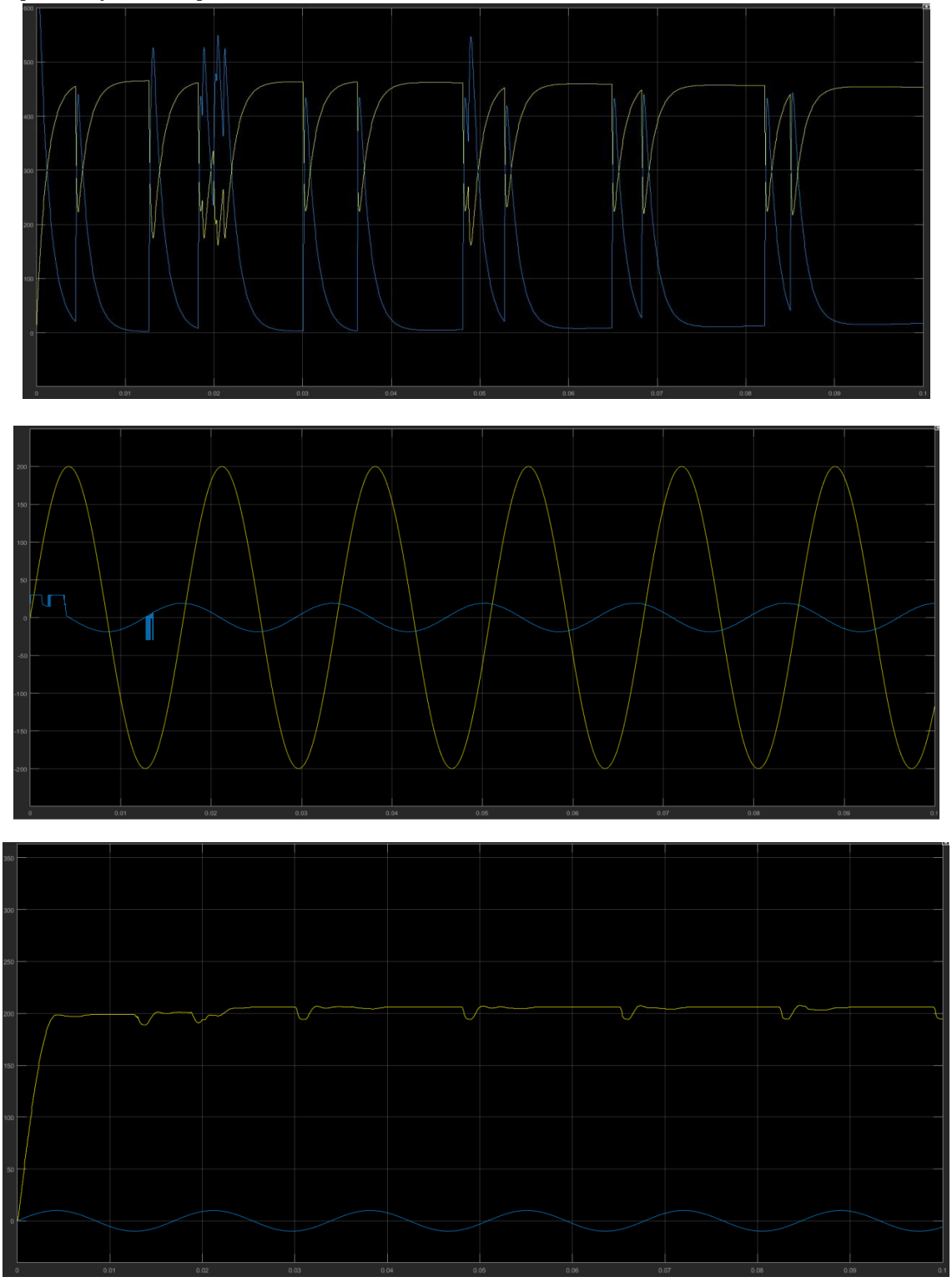

FIGURE 10. Input and output converter voltage and current at full load operation

(a) Pin = 3kWatVout = 330V; (b) Pin = 470V; (c) Input converter voltage and current, transformer primary winding current Pin = 3kWatVout = 400V.

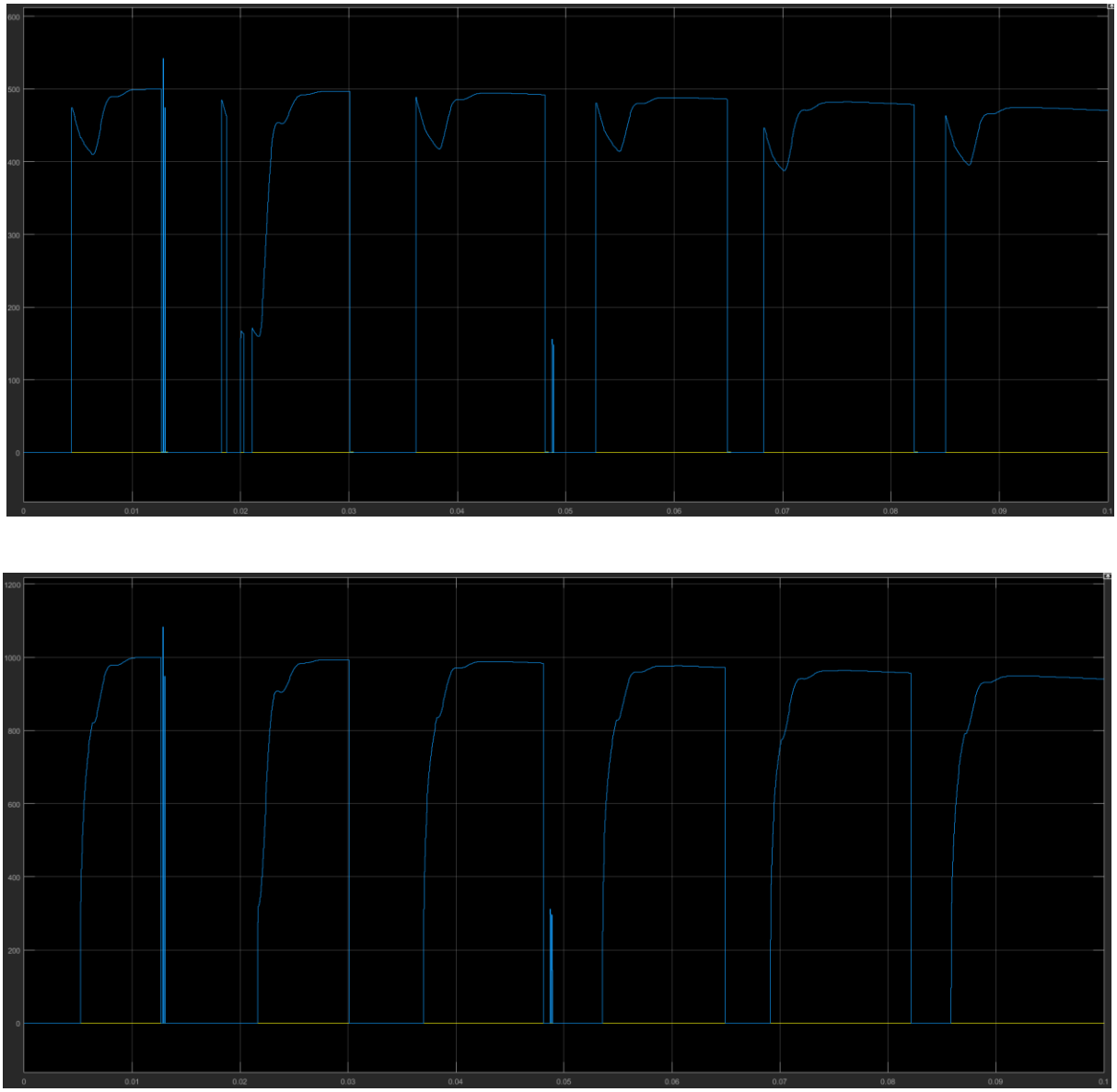

Figure 11. Transformer waveforms during a switching period

(a) Vout=400V, Pin=3kWatthesinepeakat; (b) 50% of the sine amplitude; (c) Transistor S1 voltage and current over the switching period at Vout=400V, Pin=3k.

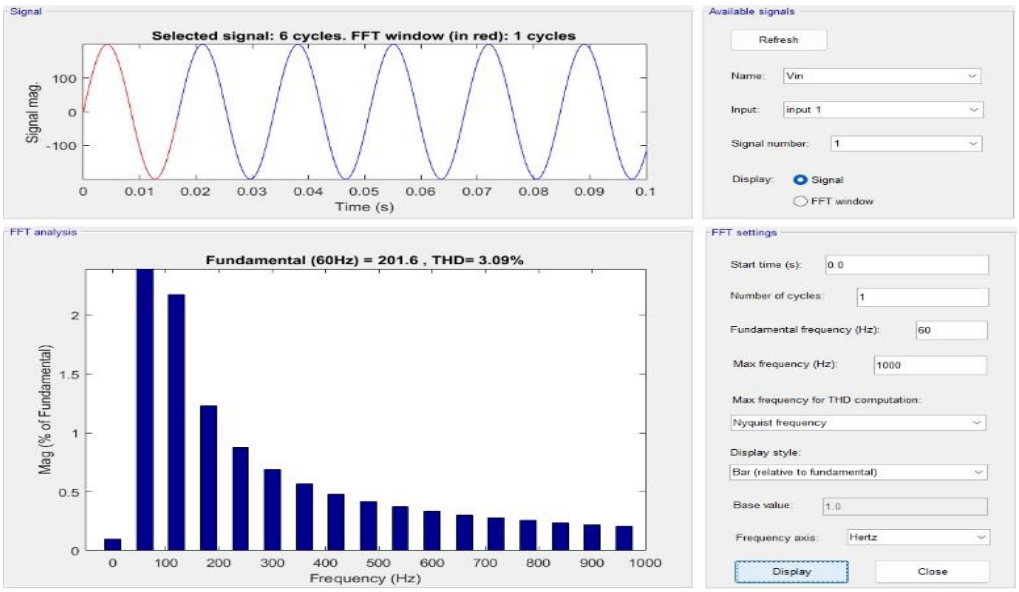

FIGURE 12.

Show 3.09% THD when operating in constant power mode at maximum power. Due to the nonlinear characteristic of the powder core input inductance (see Figure 11), the THD increases slightly near the rated power as the inductance value decreases. Figure 12 shows the input and output waveforms of the converter operating at minimum and maximum output voltage at full power, which is fully discharged and fully charged battery, respectively. The current across the primary winding of the transformer during the phase period is shown in Figure 13(c). As can be seen, due to the time-varying duration of t3-t4, the peak current across the converter follows the sine-wave input current, which reduces the associated switching and conduction losses. Figures 14(a) and (b) show the transformer voltage and current waveforms during a switching period. Unlike most resonant converters, the current across the transformer during boost mode is zero and no loop current appears, resulting in a low overall rms current stress. Figure 14(c) shows the current and voltage waveforms of switch S1 during operation at rated output power and near the sine peak Vout = 400 V. During the transistor turn-on transient, the rate of current rise is limited by the leakage inductance of the transformer and the associated power loss is minimized. Before turn-off, the current across the switch drops to zero, ensuring operation with ZCS. These soft-switching features are maintained for the full duration of the Figure 13(a) shows the ZCS operation caused by the current of transistor S2A decaying to zero. Figure 13(b) shows the voltage and current waveforms through switches S5-S8 at the peak of the sine and Figure 13(c) at a sine amplitude close to 50% of the grid voltage. In the active state, the transistors operate in synchronous rectification mode. At the end of the phase-gap, the current pulse the reverse polarity can be observed. Its amplitude is defined by the time t34 and allows the ZCS operation of the primary bridge switches. The variation of the reverse current amplitude according to the load current can be observed. Figure 16(a) shows the detailed transients of switch S1 where ZCS is observed. A small current associated with the parasitic capacitance appears at the beginning of the turn-on transient. Figure 16(b) shows the transients and ZCS turn-off of switch S2A. The ZVS turn-on transient and reverse current pulse of switch S5 are shown in Figure 16(c). Generally, most of the power during the charging process should be processed during the CP mode. Therefore, the performance characteristic in the CV mode has little impact on the overall weighted charging efficiency value. Furthermore, it is generally recommended to keep the battery charge in the range of 20…80% to increase its lifetime [25]. If this recommendation is followed, CV charging will rarely occur. This highlights that evaluating charger performance should be related to the battery charging profile.

TABLE 1. Component Parameters

COMPONENT	Symbol	Value/Type
Input diode bridge	$D_1 - D_4$	90EPF06L
Primary side transistors	$S_1 - S_{4X}$	UJ3C120080K3S
Secondary side transistors	$S_5 - S_8$	MSC035SMA070B
Filter capacitor	C_o	EZP-E50306MTA
MCU		TMS320F28335
Voltage sensors		AMC1200D
Current sensor		LTS-6-NP
Magnetics		
Input inductor L_{IN}	*Core*	T300-52D (×2)
	L_{IN}	1.7 mH
Transformer TX	*Core*	R63/38/25 (×2), N87
Turns ratio	N_1:N_2	1.03:1
Leakage inductance	L_{lk}	3.8 µH
External snubber cap.	-	680 pF

TABLE 2. Specification Of The Prototype

PARAMETERS	Symbol	Value
Rated input power	P_{in}	0.3 – 3 kW
Input voltage	V_g	207 – 253 V_{AC}
Output voltage	V_{out}	330 – 470V_{DC}
Switching frequency	f_{sw}	50 kHz
Current loop PI coef.	K_i, K_p	48[0°,90°], 95µ
Input current ripple	ΔI_{max}	1 A

The battery voltage is normalized to the maximum output voltage of a particular OBC. It is assumed that each OBC operates at its rated power during CP mode, while the power is reduced during CV mode. Obviously, the non-isolated configuration [10] showed the highest performance potential. However, such solutions have not yet been adopted in the industry due to touch currents and safety issues [12]. The proposed isolated single-stage charger showed charging characteristics close to the state-of-the-art two-stage system [32] during CP mode. Despite the lower efficiency during CV mode, the total processed energy in this mode has a relatively small effect on the total efficiency. This confirms that the proposed single-stage topology can win traction as an OBC, since it has relatively simple control, no bulky DC-coupling capacitor, and high charging efficiency.

4. CONCLUSION

This paper presented an innovative isolated single-stage on-board electric vehicle (EV) charger that utilizes a current-source topology, providing a simplified design by eliminating the need for an intermediate DC-link. Proposed chargers Smooth-switching across all semiconductors improves efficiency and reduces losses over a wide range of AC line voltages and varying load conditions. By operating without external snubber or clamp circuits, the design not only reduces component complexity but also improves system reliability. The charge uses power factor correction (PFC) and phase-shift modulation for voltage regulation, reducing circulating energy and ensuring high efficiency. A 3 kW prototype with silicon carbide (SiC) semiconductors showed a peak efficiency of 96.4%, maintained more than 95% efficiency at maximum power, and achieved a total harmonic distortion (THD) of 4.1%. Analysis of control strategies, component stresses, and design constraints confirmed the robustness of the design. Experimental results confirmed the performance of the topology, demonstrating its suitability for real-world EV applications. Additionally, the integration of an Adaptive Neuro-Fuzzy Inference System (ANFIS) controller is proposed to further improve the

performance under variable load and input conditions. This advanced control strategy improves the power factor correction and overall performance of the system, paving the way for better EV charging solutions in the future.

5. FUTURE SCOPE

Future work could focus on further improving the proposed charger design, especially in improving the performance of the ANFIS controller to be more dynamic for varying operating conditions, such as fluctuating grid voltages or highly variable EV charging requirements. The integration of advanced sensors and real-time data analytics could enable predictive charging strategies, reduce energy consumption, and improve battery life. Exploring the use of emerging semiconductor materials such as gallium nitride (GaN) could contribute to reducing losses and improving the power density of the charger, making it even more compact and efficient. Furthermore, the development of bidirectional chargers with vehicle-to-grid (V2G) integration capabilities could expand the role of EVs as energy storage systems, support grid stability, and enable smart grid capabilities. Finally, expanding the charger's scalability to support higher power levels or multiple EVs simultaneously would make this technology suitable for large-scale applications in commercial and public EV charging infrastructure, significantly contributing to the global shift towards sustainable transportation.

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